MOTOROLA

M68MM17/D2

M68MM17
Monoboard Microcomputer
Micromodule 17
User's Manual

MICROSYSTEMS

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M68MM17/D2

JUNE 1982

M68MM17

MONOBOARD MICROCOMPTER

MICROMODULE 17

USER'S MANUAL

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WARNING

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Second Edition

First Edition December 1981

SAFETY SUMMARY
SAFETY DEPENDS ON YOU

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the equipment. Motorola Inc. assumes no liability for the customer's failure to comply with these requirements. The safety precautions listed below represent warnings of certain dangers of which we are aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

GROUND THE INSTRUMENT.

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. The equipment is supplied with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter, with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the equipment in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove equipment covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

USE CAUTION WHEN EXPOSING OR HANDLING THE CRT.

Breakage of the Cathode-Ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, avoid rough handling or jarring of the equipment. Handling of the CRT should be done only by qualified maintenance personnel using approved safety mask and gloves.

DO NOT SUBSTITUTE PARTS OR MODIFY EQUIPMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the equipment. Contact Motorola Microsystems Warranty and Repair for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.

WARNING

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

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PREFACE

An asterisk (*) following the signal name for signals which are level significant denotes that the signal is true or valid when the signal is low.

An asterisk (*) following the signal name for signals which are edge significant denotes that the actions initiated by that signal occur on a high to low transition.

TABLE OF CONTENTS

TABLE OF CONTENTS (cont'd)

LIST OF ILLUSTRATIONS

LIST OF TABLES

CHAPTER 1

GENERAL INFORMATION

1.1 INTRODUCTION

Monoboard Microcomputer 17 (Micromodule 17), as shown in Figure 1-1, is a complete computer-on-a-board which will provide the user with a solution to most data processing and control applications. One of a family of micromodules, this module contains the MC6809 advanced microprocessor; five sockets for ROM's, PROM's, or RAM's; programmable serial and parallel interfaces; a programmable timer; and the required clock, restart, bus interface, and control circuitry. All address references in this manual are shown in hexadecimal, unless otherwise indicated.

NOTE

> This manual covers Micromodule 17, issue B and later. Issue A modules were covered in the previous edition of this manual, M68MM17(D1).

1.2 FEATURES

The features of Micromodule 17 include:

- EXORciser and Micromodule compatible (but not with the MC6800 DEbug module and/or MC6800-code firmware and software).
- MC6809 advanced microprocessor
  - Two 16-bit index registers.
  - Two 16-bit stack pointers (with index capability).
  - Programmable direct page register.
  - 8 x 8-bit unsigned multiply.
  - 16-bit arithmetic (load, store, add, subtract, compare).
  - Powerful push/pull and register transfer and exchange instructions.
  - Enhanced addressing modes.
- Five sockets for user-installed, single +5-volt-supply EPROM's, PROM's, mask ROM's, or RAM's (using either MOS or bipolar devices and 24- or 28-pin types).
- Two asynchronous serial data ports with strap-selectable baud rates from 75 to 9600 baud and strap-selectable RS-232C terminal or modem interface.
- Industrial I/O parallel interface port that can be configured as a fully-buffered PIA (16 data lines and four control lines).
- Triple 16-bit programmable counter/timer (MC6840 PTM).
- User-selectable Fast Interrupt Request (FIRQ) or normal Interrupt Request (IRQ) operation.

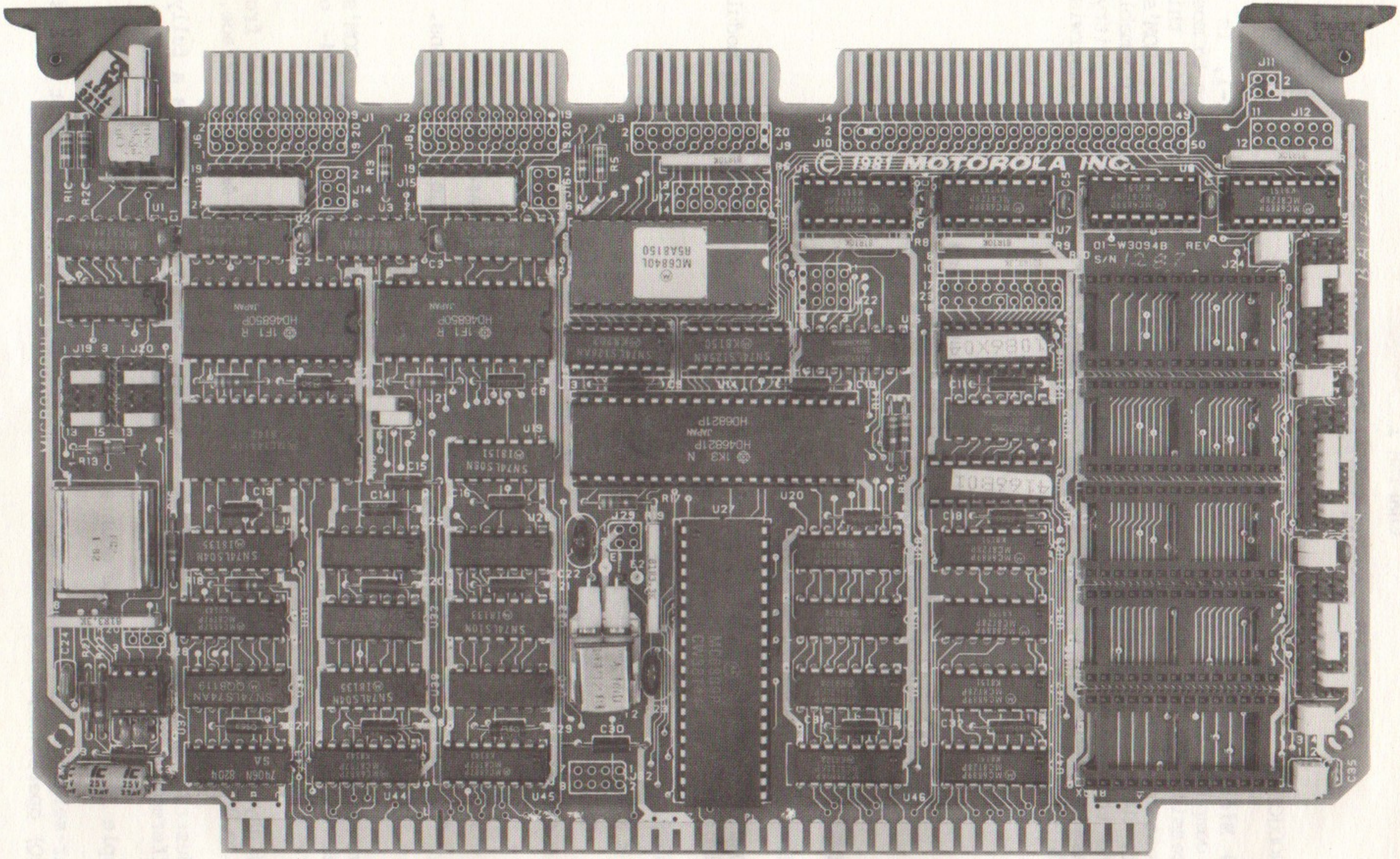


FIGURE 1-1. Monoboard Microcomputer (Micromodule 17) 5-82-1131

- Power-on and switch-controlled reset operation.
- 4-MHz crystal-controlled clock (1-MHz operation) or external clock.
- Dynamic RAM refresh control logic.
- Immediate-access, high-performance DMA control logic.
- Address, data, and control bus buffers.
- Programmable memory mapping via on-board PROM's.

1.3 SPECIFICATIONS

Micromodule 17 specifications are identified in Table 1-1.

TABLE 1-1. Micromodule 17 Specifications

CHARACTERISTICS	SPECIFICATIONS
Microprocessor	MC6809 MPU
Power requirements	
Without ROM's/PROM's	+5 Vdc at 1.5 A (max) +12 Vdc at 25 mA (max) -12 Vdc at 25 mA (max)
With five ROM's/PROM's	+5 Vdc at 2.5 A (max) +12 Vdc at 25 mA (max) -12 Vdc at 25 mA (max)
Word size and signal types	
Data	8 bits, three-state, TTL-voltage compatible signals.
Address	16 bits, three-state, TTL-voltage compatible signals.
Instructions	59 variable-length instructions (up to five bytes).
Addressing modes	Ten addressing modes: direct, relative, immediate, indexed, extended, register, inherent, extended indirect, indexed indirect, and long relative.
Clock signal	4-MHz crystal-controlled oscillator providing 1-MHz operation.

TABLE 1-1. Micromodule 17 Specifications (cont'd)

CHARACTERISTICS	SPECIFICATIONS
Memory size capability	
Total address range	64K bytes
ROM/PROM/RAM (user-supplied)	Five 24-pin/28-pin sockets on board for 2K, 4K, 8K, 16K, or 32K byte, +5V-only devices (total 10K to 62K bytes).
I/O addressing (on-board)	One MC6821 PIA with strap-selectable input/output buffering (16 data lines, four control lines).
	Two MC6850 ACIA's with selectable interface for RS-232C modem or terminal. Baud rate is selectable from 75 to 9600 baud.
	One MC6840 PTM with three 16-bit programmable binary counter/timers.
External memory	Up to 52K bytes contiguous memory available for external memory and I/O (depending on type of devices put in the five on-board memory sockets and with all five sockets enabled).
Interrupts	
Internal	NMI*, IRQ*, or FIRQ* from the PTM; IRQ* or FIRQ* from the PIA or an ACIA; SWI, SWI2, SWI3 software interrupts to the MPU.
External	IRQ* and FIRQ* maskable interrupts and NMI* non-maskable interrupt.
Operating temperature	0^{o} to 70^{o} C (component)
Physical characteristics	
Width x height	9.75 x 6.50 inches (24.77 x 16.51 cm)
Thickness	0.062 inch (0.157 cm) (board only) 0.5 inch (1.3 cm) (maximum device height)
Bus mating connector types	
Connector P1 (86-pin)	Stanford Applied Engineering SAC-43D/1-2 or equivalent.
Connectors J1, J2, and J3 (20-pin)	3M type 3461-0001 or equivalent
Connector J4 (50-pin)	3M type 3415-0001 or equivalent

1.4 GENERAL DESCRIPTION

Micromodule 17 uses the MC6809 advanced microprocessor chip, which provides the user with state-of-the-art processing capability. This 8-bit data/16-bit address MPU has a number of hardware and architectural enhancements that provide a radical throughput improvement which qualifies it for a number of tasks previously unsuited for microprocessors. These architectural enhancements also provide for low-cost software development through the use of an expanded addressing capability, position-independent (relocatable) code, and a consistent instruction set which includes 16-bit instructions.

The features of the MC6809 advanced microprocessor are further enhanced by the design of Micromodule 17. The module has five sockets in which the user may install a choice of single 5-volt supply 2K, 4K, 8K, 16K, or 32K byte EPROM's, MOS or bipolar PROM's, mask ROM's for operating firmware, or pin-compatible RAM's. The on-board memory can be accessed from an off-board controller. The module also has the timing and control logic to provide an immediate DMA response. Both parallel and serial inputs/outputs are provided on the board. The parallel I/O is shipped as a standard industrial I/O interface compatible with 16-relay boards such as the MS-16H or PB-16A. The serial I/O ports are shipped as ACIA's with user option for baud rates from 75 to 9600 baud, and for RS-232C terminal or modem interface. An MC6840 (PTM) triple, programmable, 16-bit counter/timer is included for counting or timing requirements. The module is <u>fully buffered</u> so that additional memory and I/O modules can be included in a system. If dynamic RAM is added to the system, Micromodule 17 has control logic to provide the refresh operation. Since the MC6809 MPU has the capability for both fast and normal interrupt request inputs, the module devices that generate IRQ's (PIA, ACIA, and PTM) can be strapped to either input.

Micromodule 17 is bus-compatible with the EXORciser and the Micromodule chassis, and with most of the EXORciser and Micromodule boards. It can be used with the EXORciser for software and interface development. Since Micromodule 17 is MC6809-based, any systems involving software or firmware must use MC6809-compatible programs. (For example, Micromodule 12 will not work with Micromodule 17, but Micromodules 12-1 and 12-2 will work with Micromodule 17.)

Micromodule 17 is designed for use with an optional firmware program, SUPERbug (M68MM19SB). SUPERbug is contained in EPROM's that fit into sockets on the Micromodule 17 board. SUPERbug provides a high-performance monitor routine (SUPERmon), a program linker and RAM allocation manager (SUPERlink), input/output routines (SUPERio), and related utility routines (SUPERutil). All SUPERbug routines take maximum advantage of program relocatability to efficiently and easily configure the system software.

1.5 EQUIPMENT REQUIRED

If Micromodule 17 is to be used with one or two serial data peripherals, an adapter cable is required to connect each serial interface connector (J1 and/or J2) to an RS-232C device. See Appendix A for construction details for such a cable, or purchase a three-foot long cable: M68RS232F with a female DB-25 connector, or M68RS232M with a male DB-25 connector. The female connector mates with a terminal cable; the male connector mates directly with a terminal such as an EXORterm.

CHAPTER 2

HARDWARE PREPARATION AND INSTALLATION INSTRUCTIONS

2.1 INTRODUCTION

This chapter provides the unpacking, hardware preparation, and installation procedures for Micromodule 17. This chapter discusses in detail all the factory-installed and user-installed options that have been incorporated into the design of this module.

2.2 UNPACKING INSTRUCTIONS

NOTE

If shipping carton is damaged upon receipt, request carrier's agent be present during unpacking and inspection of equipment.

Unpack Micromodule 17 from shipping carton. Refer to packing list and verify that all items are present. Save packing material for storing and reshipping the equipment.

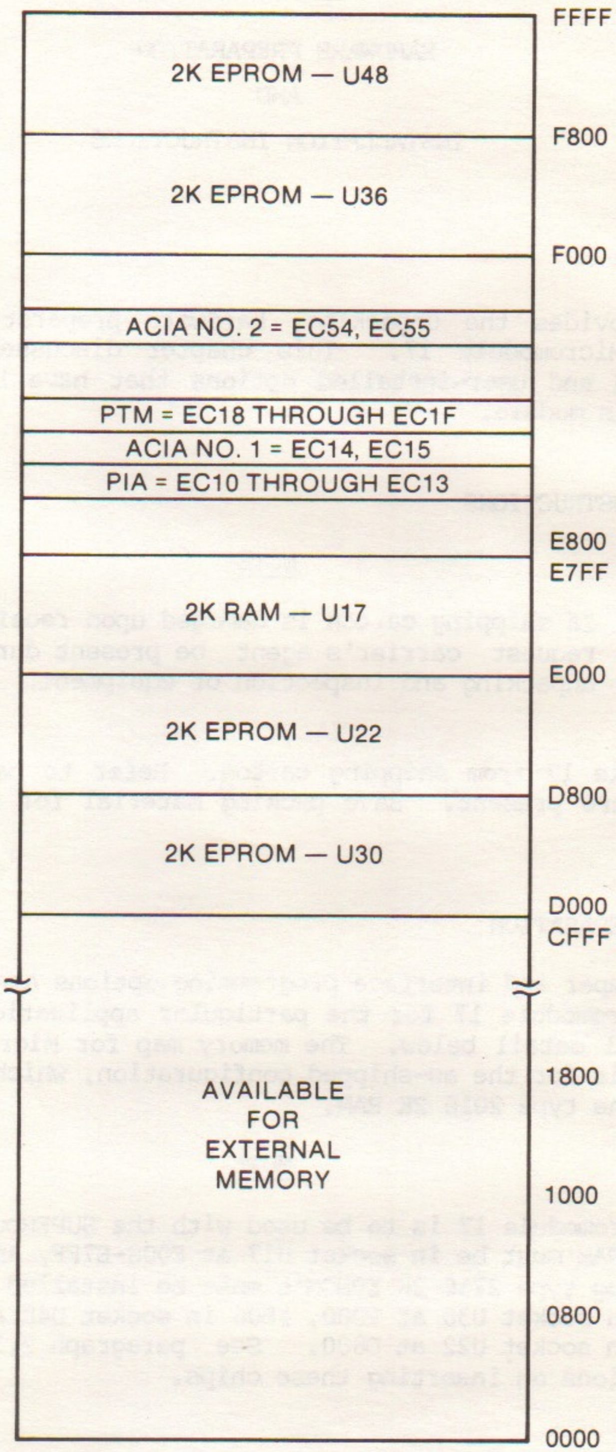
2.3 HARDWARE PREPARATION

Many hardware jumper and interface programming options are available to the user to configure Micromodule 17 for the particular application desired. These are described in full detail below. The memory map for Micromodule 17 is shown in Figure 2-1. It is for the as-shipped configuration, which is for four type 2716 2K EPROM's and one type 2016 2K RAM.

NOTE

If Micromodule 17 is to be used with the SUPERbug firmware, 2K of RAM must be in socket U17 at E000-E7FF, and the three SUPERbug type 2716 2K EPROM's must be installed as follows: #B05 in socket U36 at F000, #B06 in socket U48 at F800, and #B07 in socket U22 at D800. See paragraph 2.3.12 for instructions on inserting these chips.

In 27 areas of the module, there are jumper areas. The most commonly used jumpers have headers installed. Other less commonly used jumpers have pads provided for user-installed jumper wires or clips and/or headers. The user can also install two stud terminals. See Figure 2-2 for jumper and header locations. Detailed hardware preparation instructions follow.



NOTE

MEMORY AND PERIPHERAL LOCATIONS SHOWN ARE AS-DELIVERED, AND CAN BE CHANGED BY JUMPER SELECTION OR PROM REPLACEMENT.

FIGURE 2-1. Micromodule 17 Memory Map

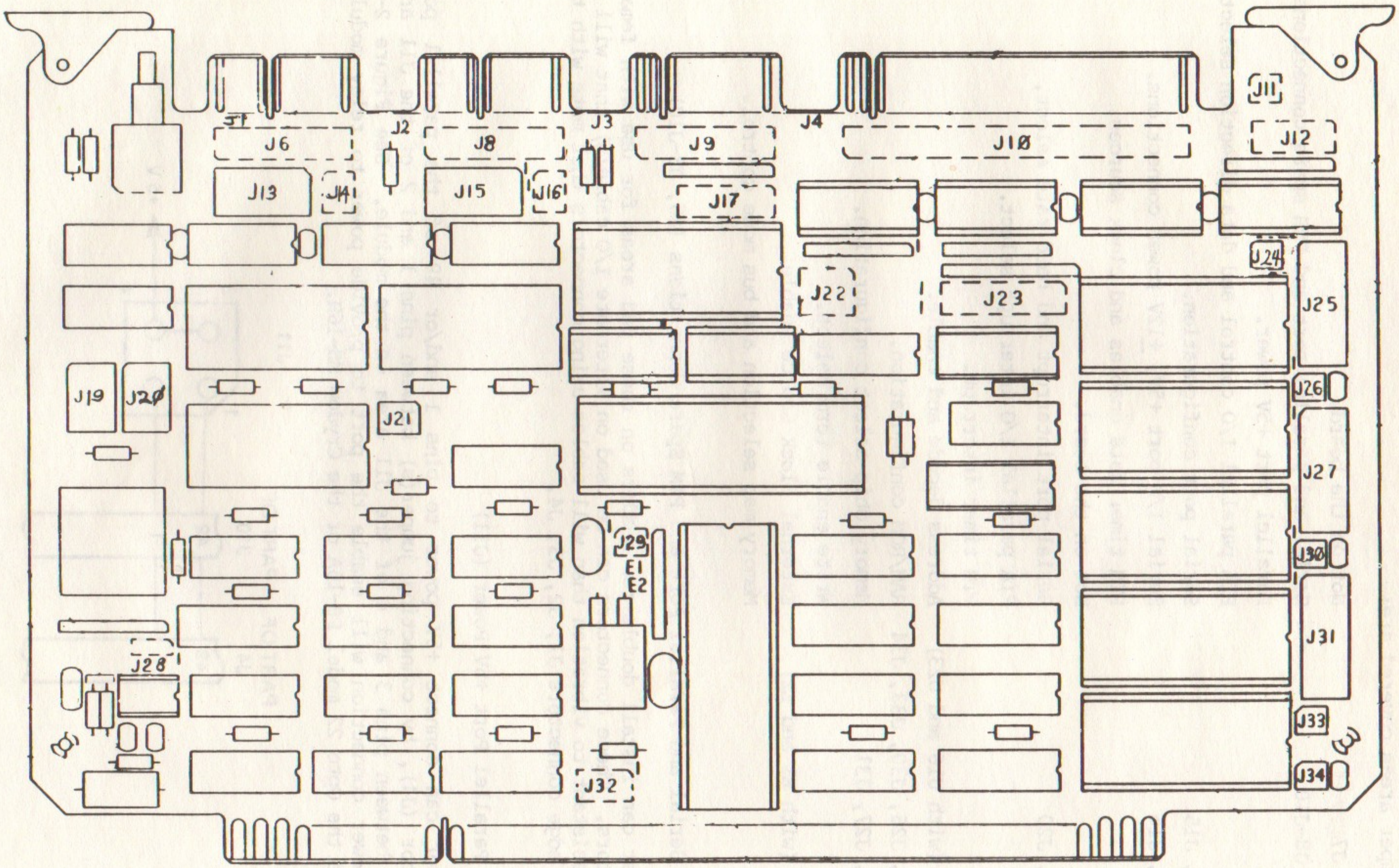


FIGURE 2-2. Micromodule 17 Jumper and Header Locations

The jumper areas covered are:

J5, J7	Not on the board.
J6, J8-J10	Serial and parallel port and PTM spare connections.
J11	Parallel port +5V power.
J12	PIA parallel I/O control and data direction selects.
J13, J15	Serial port configuration.
J14, J16	Serial I/O port +5V, ±12V power connections.
J17	PTM timer gate enables and clock sources.
J18	Not on the board.
J19, J20	Serial port interrupt and baud rate select.
J21	PIA parallel I/O interrupt select.
J22	PTM timer interrupt.
J23 (with U16 and U23)	Address decode and enable.
J24, J26, J30, J33, J34	RAM/ROM configuration.
J25, J27, J31	Memory chip select configuration.
J28	Write enable term select.
J29 (with E1 and E2)	External clock source enable.
J32	Memory map selection and bus mode control.

2.3.1 Serial and Parallel Port and PTM Spare Connections (J6, J8-J10)

The user can install double-row headers on these pad areas for use with female connectors. These connectors can be used on alternate I/O cable(s) that will be more resistant to vibration than will cables using connectors that mate with the module edge connectors J1, J2, J3, J4.

2.3.2 Parallel Port +5V Power (J11)

The user can connect +5V power to pins 1 and/or 49 of the parallel port connector (J4), by connecting jumper(s) between pins 1 and 2 of the J11 area and/or between pins 3 and 4 of the J11 area on the module. See Figure 2-3. This power connection will enable the port to provide power to relay modules such as the Opto 22 model PB-16A or the Crydom MS-16H.

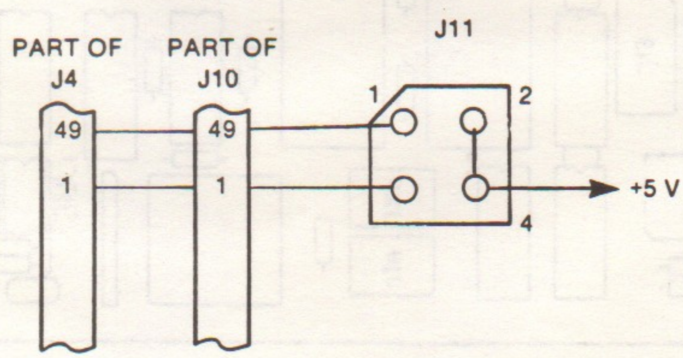


FIGURE 2-3. Parallel Port +5V Power Jumpers

2.3.3 PIA Parallel I/O Control and Data Direction Selects (J12)

J12 is an area on the module where the user may install a header or jumpers to control the direction of control lines CA2 and CB2 and of data lines PA0-PA7 and PB0-PB7 from the Peripheral Interface Adapter (PIA). See Figure 2-4. For each of the six pairs of pins, if a jumper is in, the line is forced to ground, and the particular function is an input. If the jumper at the pair of pins is out (not there), the line goes high, and the function is an output. The as-delivered configuration is with pins 1 and 2 open (PA4-PA7 are outputs), pins 3 and 4 open (PA0-PA3 are outputs), pins 5 and 6 jumpered (PB0-PB3 are inputs), pins 7 and 8 jumpered (PB4-PB7 are inputs), pins 9 and 10 open (CA2 is an output), and pins 11 and 12 open (CB2 is an output). Note that the two control lines can be configured separately, but that the data lines can be configured only in groups of four.

Refer to paragraph 2.3.8 for configuring interrupts from the PIA.

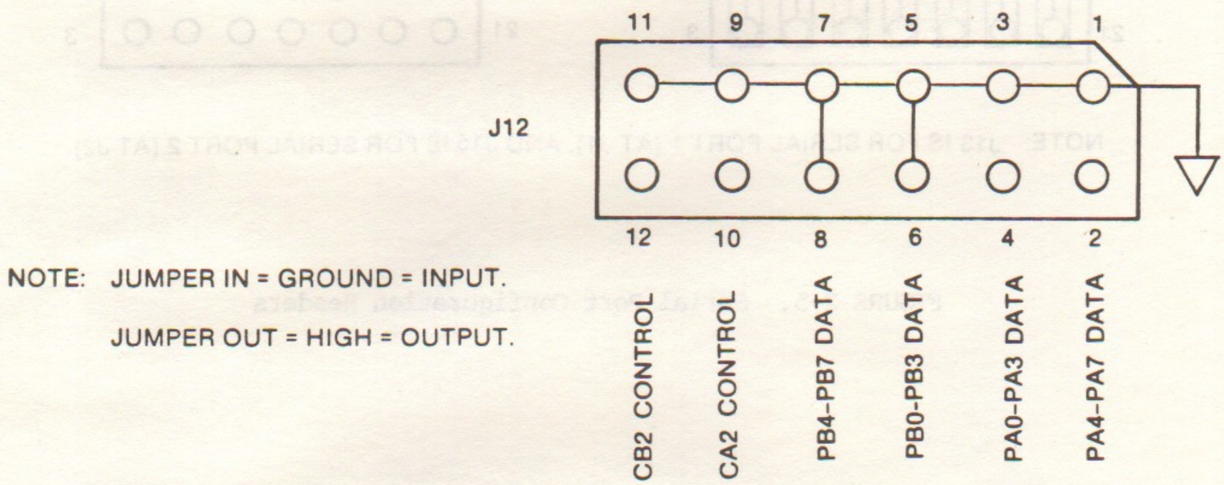
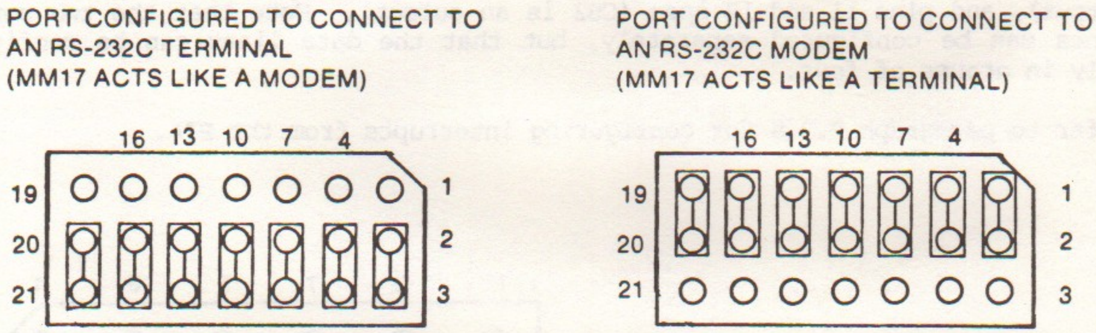


FIGURE 2-4. PIA Control and Data Direction Selects

2.3.4 Serial Port Configuration Headers (J13, J15)

J13 and J15 are factory-supplied headers used to configure the serial ports to work with an RS-232C terminal or a modem (that is, to act as a modem or a terminal, respectively). The module is delivered with both ports set up to work with a terminal. See Figure 2-5.



NOTE: J13 IS FOR SERIAL PORT 1 (AT J1), AND J15 IS FOR SERIAL PORT 2 (AT J2).

FIGURE 2-5. Serial Port Configuration Headers

2.3.5 Serial I/O Port +5V, ±12V Power Connections (J14, J16)

The as-delivered jumpers associated with the serial port connectors J1 and J2 provide standard RS-232C signals. There are no non-standard voltages present. If it is desired to use the remote serial conversion module M68RSC1 for RS-449 operation, or to use Micromodule 11 to obtain a 20-mA current loop interface, the user can connect additional jumpers as follows. (M68RSC2 has its own power supply and does not need power from MM17.)

CAUTION

IF THESE JUMPERS ARE INSTALLED, A STANDARD RS-232C DEVICE SHOULD NOT BE CONNECTED, SINCE ELECTRICAL DAMAGE COULD OCCUR.

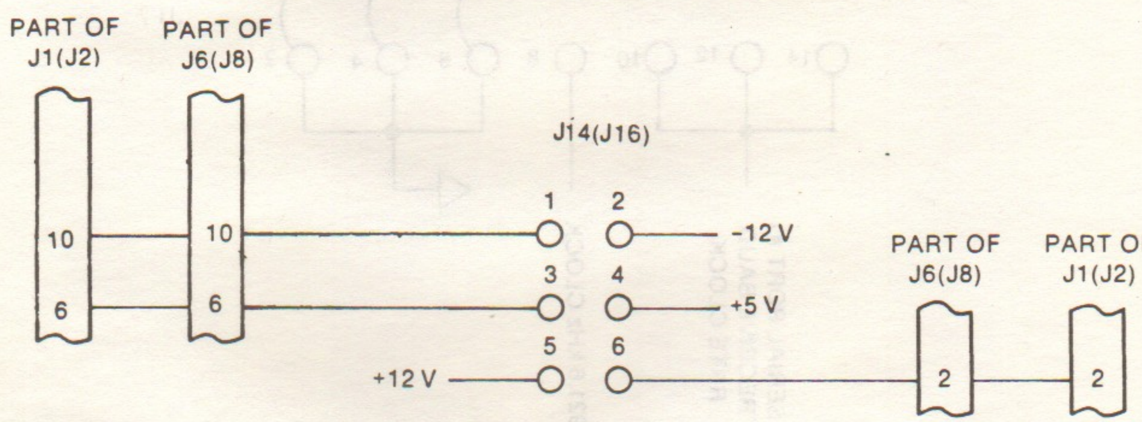
For use with the remote serial conversion module M68RSC1 for RS-449 operation, the user can connect +5V, +12V, and -12V power to either or both serial port edge connectors (J1, J2) and the on-board connector areas (J6, J8) by using pad areas J14 and/or J16. The board is delivered with none of these connections made. See Figure 2-6 for details.

NOTE

If MM17 is connected to Micromodule 11 for use with a 20-mA TTY-type unit, the power connections to J1 and/or J2 on MM17 must be +5V to pin 16, -12V to pin 18, and +12V to pin 20, instead of the connections described and shown here.

CAUTION

SOME ISSUE B BOARDS HAVE PINS 6 AND 17 OF J6 (AND PINS 6 AND 17 OF J8) WIRED TOGETHER. THESE BOARDS ALSO HAVE PINS 4 AND 19 OF J6 (AND PINS 4 AND 19 OF J8) WIRED TO GROUND. DO NOT CONNECT A STANDARD RS-232C DEVICE TO SUCH BOARDS, BECAUSE ELECTRICAL DAMAGE COULD RESULT.



NOTE

THE PAD OR JUMPER DESIGNATORS GIVEN IN PARENTHESES ARE USED WITH CONNECTOR J2; THOSE NOT IN PARENTHESES ARE USED WITH CONNECTOR J1.

FIGURE 2-6. Serial I/O Port +5V, ±12V Power Connections

2.3.6 PTM Timer Gate Enables and Clock Sources (J17)

J17 is an area on the board where the user can select gate enable inputs and clock inputs, all for the MC6840 Programmable Timer Module (PTM), which is U5.

Copper traces on the board connect pairs of pins on J17. These connections tie the three timer gate inputs (gate 1, gate 2, gate 3) to ground, enabling the three timers in the PTM. To allow external enable for any one of the timers, cut the copper trace. (See Figure 2-7.) This will force the gate input to +5 Vdc, disabling that timer or allowing the user to supply the gate inputs. The user can provide these three signals at edge connector J3, pins 1, 7, and 13, respectively. The as-delivered configuration is with all three timers enabled by the on-board traces.

The other four pairs of pins on J17 are for the PTM timer clock source selection. Normal input clock for all three timers is internally from E, the system enable signal. However, the receiver clock output of the baud rate generator, as sent to serial port number 1, may be used for PTM clock input 1, 2, and/or 3 by jumpering J17 pins 13 and 14 (for clock 1), pins 11 and 12 (for clock 2), and/or pins 9 and 10 (for clock 3). Alternatively, the third timer may be run by the 921.6 kHz output of the baud rate generator, by jumpering J17 pins 7 and 8. (Refer to paragraph 2.3.7 for baud rate selection.) The as-delivered configuration is with no external timer source.

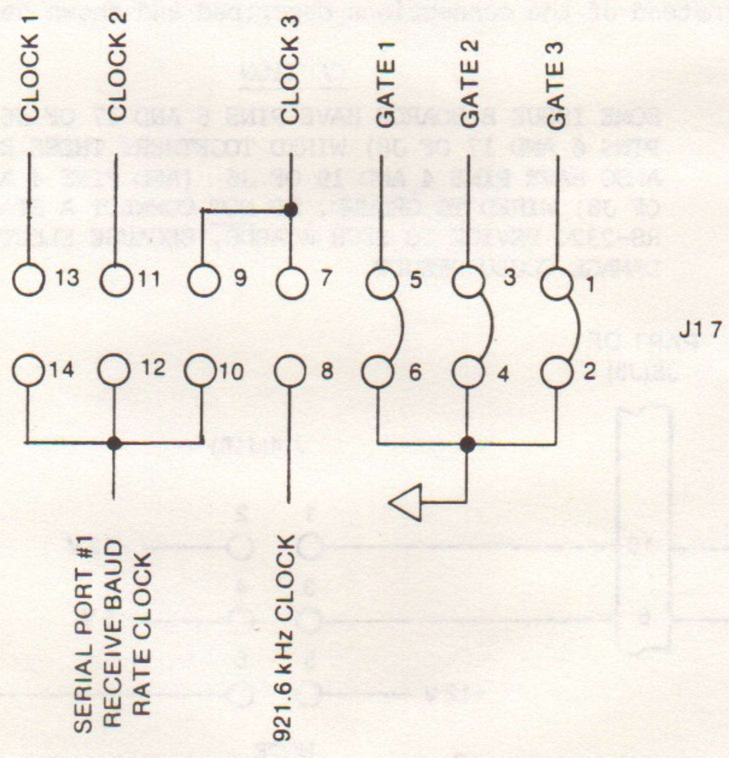


FIGURE 2-7. PTM Timer Gate Enables and Clock Sources

2.3.7 Serial Port Interrupt and Baud Rate Select Headers (J19, J20)

J19 and J20 are headers on the module for selecting baud rates and interrupt outputs for serial ports 1 and 2, respectively. The as-delivered configuration is with each header set for 300 baud (pins 5 and 6 jumpered) for both TXC and RXC, and with interrupt output connected to IRQ* (pins 14 and 15 jumpered). See Figure 2-8.

Normally, a single baud rate is selected for both transmit clock and receive clock (TXC and RXC) inputs for a serial port. This can be done easily by a jumper clip on J19 for port 1 and another on J20 for port 2. The baud rates for the two ports need not be the same. If the user wants different baud rates for TXC and RXC on the same port, the user must cut the copper trace somewhere between pins 2 and 11 of the header, then wire wrap pins 2 and 11 to the baud rate pins desired for TXC and RXC, respectively.

J19 and J20 also control the interrupt outputs from the serial ports. The user can connect header pins 13 and 14 for FIRQ* or header pins 14 and 15 for IRQ*, but must not connect both.

J19 FOR SERIAL PORT #1, J20 FOR SERIAL PORT #2

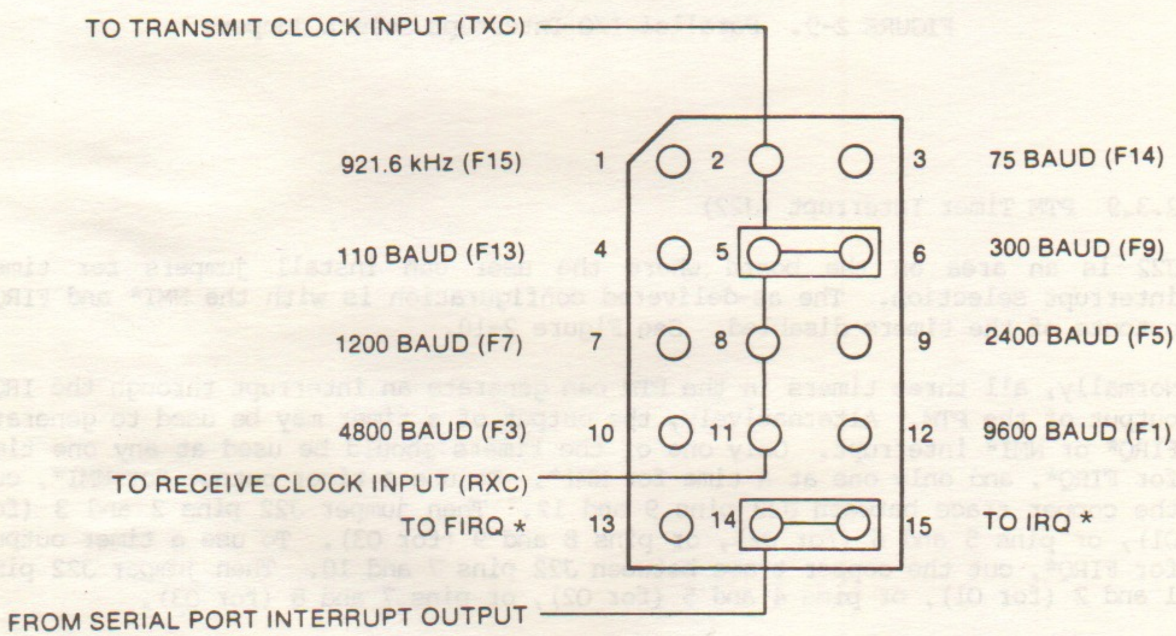


FIGURE 2-8. Serial Port Interrupt and Baud Rate Select Headers

2.3.8 PIA Parallel I/O Interrupt Select (J21)

J21 is a header on the board used to connect either the normal interrupt (IRQ*) or the fast interrupt (FIRQ*) to the two sides of the PIA. Either interrupt (or none) may be connected to each side of the PIA, independently. The as-delivered configuration is with IRQA connected to IRQ*, and IRQB connected to FIRQ*. See Figure 2-9. To connect IRQ* to the A side of the PIA, jumper pins 3 and 5; to connect IRQ* to the B side, jumper pins 4 and 6. To connect FIRQ* to the A side of the PIA, jumper pins 1 and 3; to connect FIRQ* to the B side, jumper pins 2 and 4. Do not connect more than one interrupt to either side of the PIA. Refer to paragraph 2.3.3 for configuring PIA control and data signals.

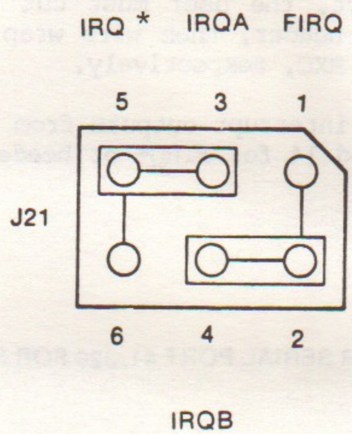


FIGURE 2-9. Parallel I/O Interrupt Select Jumpers

2.3.9 PTM Timer Interrupt (J22)

J22 is an area on the board where the user can install jumpers for timer interrupt selection. The as-delivered configuration is with the NMI* and FIRQ* outputs of the timers disabled. See Figure 2-10.

Normally, all three timers in the PTM can generate an interrupt through the IRQ* output of the PTM. Alternatively, the output of a timer may be used to generate FIRQ* or NMI* interrupt. Only one of the timers should be used at any one time for FIRQ*, and only one at a time for NMI*. To use a timer output for NMI*, cut the copper trace between J22 pins 9 and 12. Then jumper J22 pins 2 and 3 (for O1), or pins 5 and 6 (for O2), or pins 8 and 9 (for O3). To use a timer output for FIRQ*, cut the copper trace between J22 pins 7 and 10. Then jumper J22 pins 1 and 2 (for O1), or pins 4 and 5 (for O2), or pins 7 and 8 (for O3).

The three timers may be cascaded for longer time delays by connecting the output of one to the clock input of the next, at jumper areas J17 and J22. Use J22 pin 2 for O1, J22 pin 5 for O2, J22 pin 8 for O3. Use J17 pin 13 for C1, J17 pin 11 for C2, J17 pin 7 or 9 for C3. For details, refer to the MC6840 Programmable Timer Fundamentals and Applications Manual.

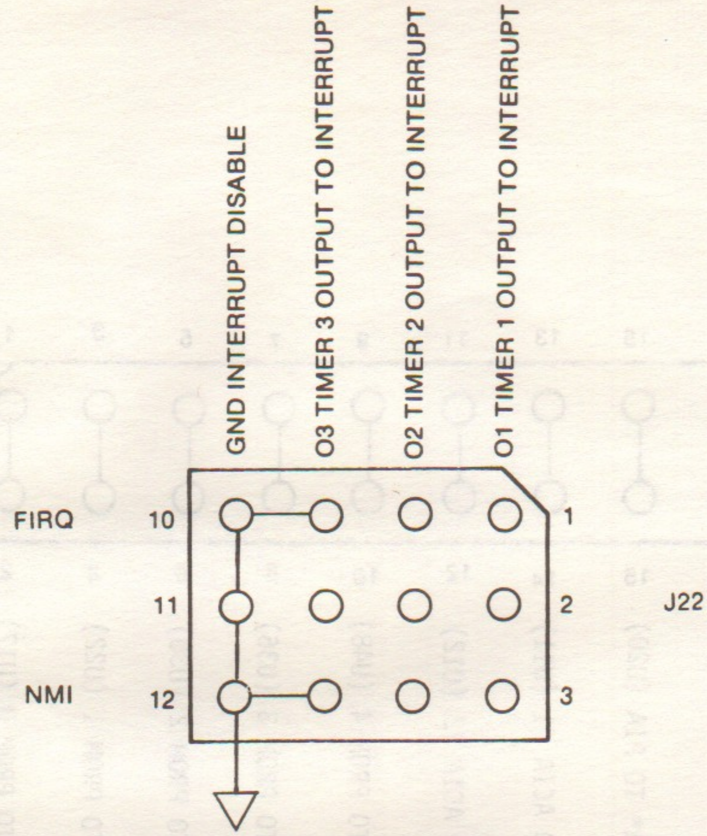


FIGURE 2-10. PTM Timer Interrupt Jumpers

2.3.10 Address Decode and Enable (J23, U16, U23)

The address decode and enable area J23 and the PROM's U16 and U23 on the board work together to assign addresses to the peripheral and memory chips on board, and to enable or disable their operation. (See Figure 2-1 for the Micromodule 17 memory map.)

J23 involves 9 jumpers and has copper traces on the board. The jumpers are in two groups: the last four select the ACIA's, PIA, and PTM; the first five enable or disable the memories. The as-shipped configuration is with all the copper traces intact so that the peripherals are located at EC10 through EC1F and EC54 and EC55, and all peripherals and memories enabled. This is the mapping shown in Figure 2-1, and J23 is as shown in Figure 2-11.

Cutting any of the traces will disable the device indicated in Figure 2-11, and will free that portion of memory for off-board use. To disable all the I/O peripherals, remove U23. To disable all the peripherals and all the memory chips on board, remove U16.

For example, Micromodule 17 could be used in an EXORciser, with the DEbug module being used for system software debugging. The user would have to disable sockets U36 and U48 on MM17 to avoid conflict with EXbug, which resides at addresses F000-FFFF. To send the VMA signal to the DEbug module, the user should then cut the trace between J32 pins 5 and 6, and install a jumper between J32 pins 7 and 8. (Refer to paragraph 2.3.15 for more on J32.)

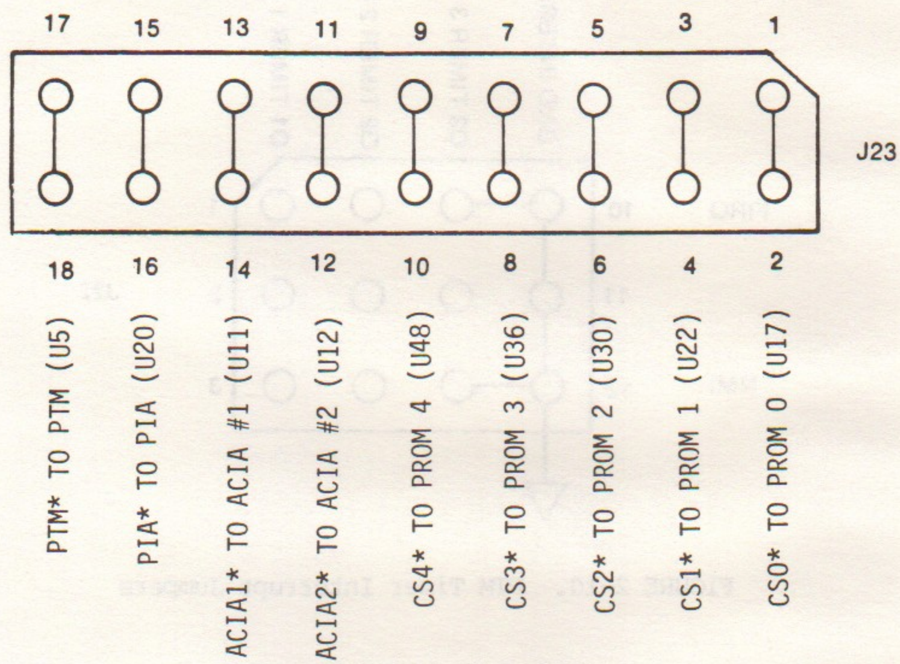


FIGURE 2-11. Address Decode and Enable Jumpers

PROM U16 is a type 82S123 or SN74S288, and PROM U23 is a type 82S137 or HM3-7643-5. These devices are programmed to give the memory and peripheral addresses (as shown in Figure 2-1). Tables 2-1 and 2-2 list the detailed inputs for the programmed PROM's. Note that the data or output terms are active low. Lines not given in the tables have consecutive addresses increasing by one, and the same data as the last line previously given.

The user must program a new PROM to replace U16, when using 4K x 8, 8K x 8, 16K x 8, or 32K x 8 devices in any or all of the five on-board sockets. To program another PROM or PROM's, use the same form as shown in Table 2-1, but select the necessary address and data combinations.

TABLE 2-1. PROM U16 as Programmed for Micromodule 17

6809 ADDRESS	A15	A14	A13	A12	A11	0	I/O	1	CS4*	CS3*	CS2*	CS1*	CS0*	6809	PROM	PROM
PROM ADDRESS	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	ADDRESS	ADDRESS	DATA
	0	0	0	0	0	0	1	1	1	1	1	1	1	0000	00	7F
U30-2K EPROM	1	1	0	1	0	0	1	1	1	1	0	1	1	D000	1A	7B
U22-2K EPROM	1	1	0	1	1	0	1	1	1	1	1	0	1	D800	1B	7D
U17-2K RAM	1	1	1	0	0	0	1	1	1	1	1	1	0	E000	1C	7E
I/O BLOCK EN	1	1	1	0	1	0	0	1	1	1	1	1	1	E800	1D	3F
U36-2K EPROM	1	1	1	1	0	0	1	1	1	0	1	1	1	F000	1E	77
U48-2K EPROM	1	1	1	1	1	0	1	1	0	1	1	1	1	F800	1F	6F

NOTES:

1. CS0* = U17, CS1* = U22, CS2* = U30, CS3* = U36, CS4* = U48.
2. Lines not given in the table have consecutive addresses increasing by one, and the same data as the last line previously given.

TABLE 2-2. PROM U23 as Programmed for Micromodule 17

6809 ADDRESS	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	PTM	PIA	ACIA NO.1	ACIA NO.2			
PROM ADDRESS	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	O4	O3	O2	O1	6809 ADDRESS	PROM ADDRESS	PROM DATA
	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0000	000	F
					↓									↓	↓	↓	↓
PIA	1	0	0	0	0	0	1	0	0	0	1	0	1	1	EC10,11	208	B
PIA	1	0	0	0	0	0	1	0	0	1	1	0	1	1	EC12,13	209	B
ACIA#1	1	0	0	0	0	0	1	0	1	0	1	1	0	1	EC14,15	20A	D
	1	0	0	0	0	0	1	0	1	1	1	1	1	1	EC16,17	20B	F
PTM	1	0	0	0	0	0	1	1	0	0	0	1	1	1	EC18,19	20C	7
PTM	1	0	0	0	0	0	1	1	0	1	0	1	1	1	EC1A,1B	20D	7
PTM	1	0	0	0	0	0	1	1	1	0	0	1	1	1	EC1C,1D	20E	7
PTM	1	0	0	0	0	0	1	1	1	1	0	1	1	1	EC1E,1F	20F	7
	1	0	0	0	0	1	0	0	0	0	1	1	1	1	EC20,21	210	F
					↓									↓	↓	↓	↓
	1	0	0	0	1	0	1	0	0	1	1	1	1	1	EC52,53	229	F
ACIA#2	1	0	0	0	1	0	1	0	1	0	1	1	1	0	EC54,55	22A	E
	1	0	0	0	1	0	1	0	1	1	1	1	1	1	EC56,57	22B	F
					↓									↓	↓	↓	↓
	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF	3FF	F

NOTES:

1. PIA at \$EC10-EC13, ACIA#1 at \$EC14-EC15, PTM at \$EC18-EC1F, ACIA#2 at\$EC54-EC55.
2. Lines not given in the table have consecutive addresses increasing by one, and the same data as the last line previously given.

2.3.11 RAM/ROM Configuration (J24, J26, J30, J33, J34)

These five headers on the board work with three large headers (J25, J27, J31) to configure the five on-board memory sockets (U17, U22, U30, U36, U48). The five small headers -- J24, J26, J30, J33, J34 -- each configure one socket to be used for RAM or ROM. See Figure 2-12 for the only two permitted configurations of these headers. Then refer to Table 2-3 for a list of which headers control which socket(s). Note that J26 and J30 must be set the same way, as must J33 and J34, but that each pair of headers can differ from the other pair, or from J24. When these five headers are properly jumpered, configure the three large headers for the specific type of memory devices you want to use on the board, then install the devices. Refer to paragraph 2.3.12 for full details.

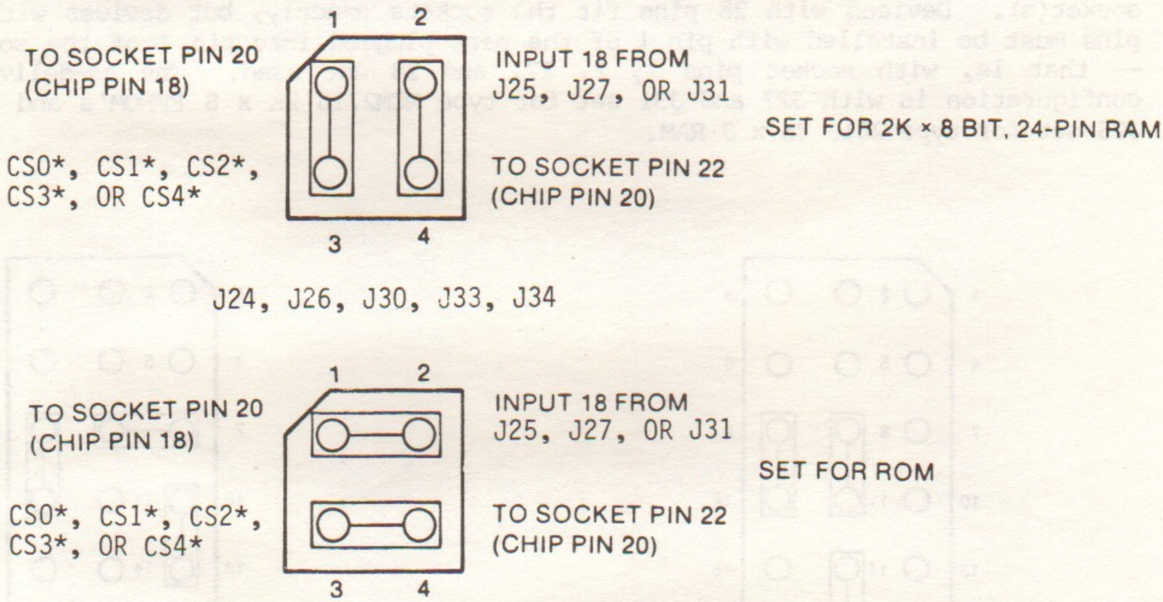


FIGURE 2-12. RAM/ROM Configuration Headers

TABLE 2-3. On-Board Memory Selection and Configuration Headers

RAM/ROM CONFIGURATION HEADER	CHIP SELECT SIGNAL	MEMORY SOCKET CONTROLLED	CHIP CONFIGURATION HEADER (1)	AS-DELIVERED RAM/ROM CONFIGURATION
J33	CS3*	U36	J31	ROM (2)
J34	CS4*	U48	J31	ROM (2)
J24	CS0*	U17	J25	RAM
J30	CS2*	U30	J27	ROM (2)
J26	CS1*	U22	J27	ROM (2)

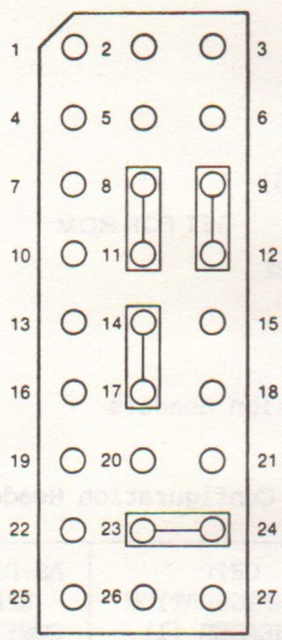
NOTES:

(1) Refer to paragraph 2.3.12 for details on configuring these headers.

(2) J26 and J30 must both be set for ROM or both set for RAM. J33 and J34 must both be set for ROM or both set for RAM.

2.3.12 Memory Chip Socket Configuration (J25, J27, J31)

Headers J25, J27, and J31 (see Figure 2-13) configure the five memory chip sockets on Micromodule 17 for specific types of RAM, ROM, PROM, or EPROM. First decide whether you want RAM or ROM for the socket(s) and set the jumpers in the five small headers (J24, J26, J30, J33, J34) per paragraph 2.3.11. Then set up the jumpers in the three large headers (J25, J27, J31) for the exact device type wanted, per Figure 2-13. The type(s) chosen must be consistent with the jumpering of the small headers. The user must program a new PROM to replace address decoder PROM U16, when using 4K x 8, 8K x 8, 16K x 8, or 32K x 8 devices in any or all of the five on-board sockets. Refer to paragraph 2.3.10 and Table 2-1 for details of U16 programming. Finally, install the device(s) in the socket(s). Devices with 28 pins fit the sockets exactly, but devices with 24 pins must be installed with pin 1 of the part plugged into pin 3 of the socket -- that is, with socket pins 1, 2, 27, and 28 not used. The as-delivered configuration is with J27 and J31 set for type MCM2716 2K x 8 EPROM's and with J25 set for type 2016 2K x 8 RAM.

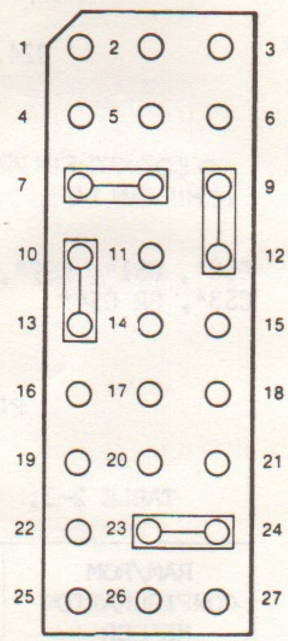


J27 CONFIGURATION HEADER FOR MEMORY SOCKETS U22 AND U30

OR

J31 CONFIGURATION HEADER FOR MEMORY SOCKETS U36 AND U48

— SHOWN SET FOR 24-PIN, 2K × 8 BIT EPROM, TYPE MCM2716



J25 CONFIGURATION HEADER

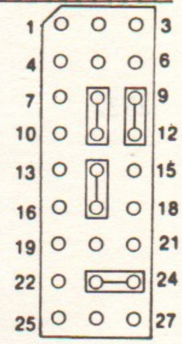
FOR MEMORY SOCKET U17

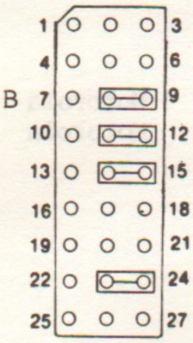
— SHOWN SET FOR 24-PIN

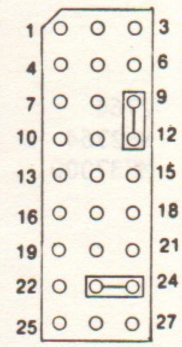
2K × 8 BIT RAM, TYPE 2016

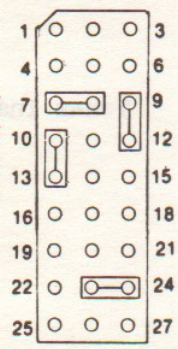
FIGURE 2-13. Memory Chip Socket Configuration (Sheet 1 of 4)

PART NUMBER	MANUFACTURER	TYPE	SIZE	NUMBER OF PINS	JUMPER ARRANGEMENT AND LETTER
MCM2716	Motorola	EPROM	2K x 8	24	A
MCM68A316E	Motorola	ROM	2K x 8	24	A
82S191	Signetics	PROM	2K x 8	24	B
HM-7616	Harris	PROM	2K x 8	24	C
TMM2016	Toshiba	RAM	2K x 8	24	N
TMS4016	Texas Instr.	RAM	2K x 8	24	N
MK4802	Mostek	RAM	2K x 8	24	N
21R1	Intel	RAM	2K x 8	24	N
MCM2532	Motorola	EPROM	4K x 8	24	D
MCM68A332	Motorola	ROM	4K x 8	24	D









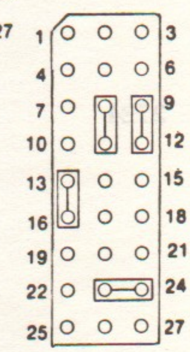


FIGURE 2-13. Memory Chip Socket Configuration (Sheet 2 of 4)

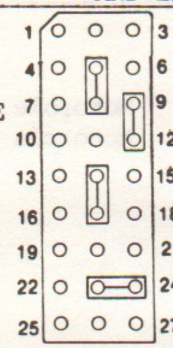
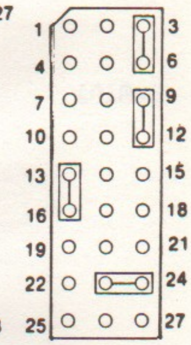
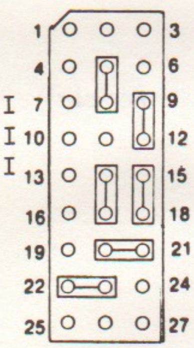
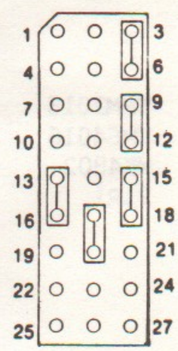
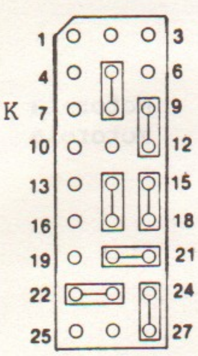
PART NUMBER	MANUFACTURER	TYPE	SIZE	NUMBER OF PINS	JUMPER ARRANGEMENT AND LETTER
2732	Intel	EPROM	4K x 8	24	E 
MCM68764	Motorola	EPROM	8K x 8	24	F 
MCM68A364	Motorola	ROM	8K x 8	24	F
2764	Intel	EPROM	8K x 8	28	I 
MK2764	Mostek	EPROM	8K x 8	28	I
MK37000	Mostek	ROM	8K x 8	28	I
TMS2564	Texas Instr.	EPROM	8K x 8	28	J 
27E4	Intel	EPROM	16K x 8	28	K 

FIGURE 2-13. Memory Chip Socket Configuration (Sheet 3 of 4)

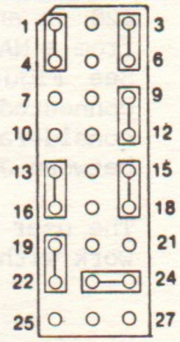
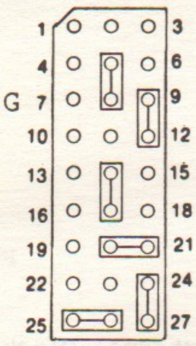
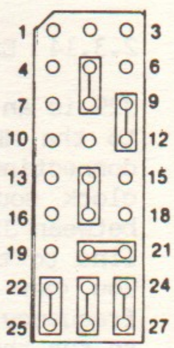
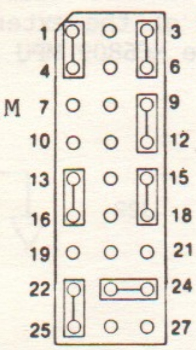
PART NUMBER	MANUFACTURER	TYPE	SIZE	NUMBER OF PINS	JUMPER ARRANGEMENT AND LETTER
(to be supplied)	Texas Instr.	EPROM	16K x 8	28	L 
(to be supplied)	Mostek	EPROM	32K x 8	28	G 
27E5	Intel	EPROM	32K x 8	28	H 
(to be supplied)	Texas Instr.	EPROM	32K x 8	28	M 

FIGURE 2-13. Memory Chip Socket Configuration (Sheet 4 of 4)

2.3.13 Write Enable Term Select (J28)

J28 is an area on the board that adds or removes the quadrature clock signal Q from a NAND gate that generates the Write Enable (WE*) signal for on-board RAM. See Figure 2-14. The as-delivered configuration is with J28 pins 1 and 2 connected, which connects Q to the NAND gate. The user can remove Q from WE* consideration by cutting the trace between J28 pins 1 and 2 and adding a jumper between J28 pins 2 and 3. This will tie that input of the NAND gate to +5 Vdc.

The user should remove the Q signal only for memories so slow that they cannot work within the quarter-cycle time when E and Q are both high.

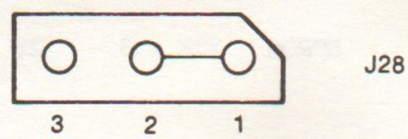


FIGURE 2-14. Write Enable Term Select

2.3.14 External Clock Source Enable (J29, E1, E2)

J29 is an area on the board that can be used to connect an external clock source to the MPU. As shipped, J29 has pins 3 and 4 connected by a copper trace, connecting the biasing circuitry for Y2. See Figure 2-15. To use an external clock source, cut the trace between J29 pins 3 and 4, and install a jumper between J29 pins 1 and 2. Connect the external clock and its associated ground line to the holes on the board marked EXT CLK (E2) and GND (E1), respectively. You can install turret studs in these holes for easier connections. The frequency of the external clock must be four times the speed at which you want to run the MC6809 MPU (U27).

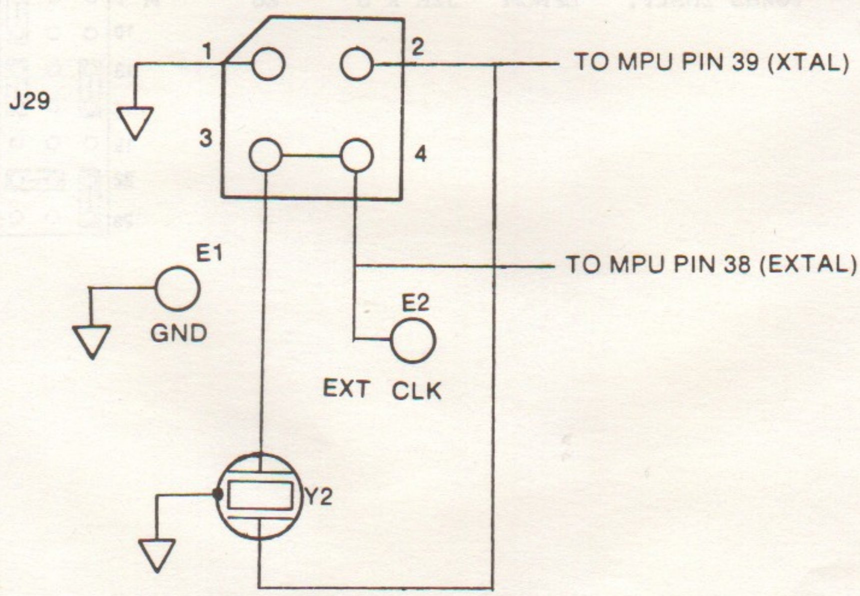


FIGURE 2-15. External Clock Selection

2.3.15 Memory Map Selection and Bus Mode Control (J32)

Micromodule 17 was designed such that it can be installed in an M6809 EXORciser, replacing the M6809 MPU module, to work with the M6809 DEbug module. This will allow the user to debug the application software before committing it to EPROM or ROM firmware. Additionally, any other system input/ouput Micromodules may also be installed in the EXORciser so that the system interfaces, including those on Micromodule 17, can be tested and debugged.

J32 is an area on the board which provides a jumper option to allow the use of Micromodule 17 in the EXORciser. See Figure 2-16. A valid memory enable signal, based on the status of the refresh grant and bus grant signals, is connected to pins 6 and 8 of J32. As shipped, this signal is connected by PC track to pin 5, which is connected to the Valid User Address (VUA) line on the system backplane. It is also connected through J32 to pin 2, which is connected to the address decode circuits on Micromodule 17. This allows Micromodule 17 to control the address decoding of the on-board memory locations and of the other modules installed in the system.

When Micromodule 17 is to be used in an EXORciser, the M6809 DEbug module must control the address decoding based on a Valid Memory Address (VMA) signal. This is accomplished by cutting the trace between J32 pins 5 and 6 and installing a jumper between J32 pins 7 and 8. This allows the VUA signal generated by the DEbug module to control the on-board address decoding. It is also possible to put the Micromodule 17 memory and I/O in the EXORciser executive map by cutting the trace between J32 pins 3 and 4 and installing a jumper between J32 pins 1 and 2. In this mode, the user must be careful to disable any on-board devices that will conflict with the EXORciser executive map. See paragraph 2.3.10.

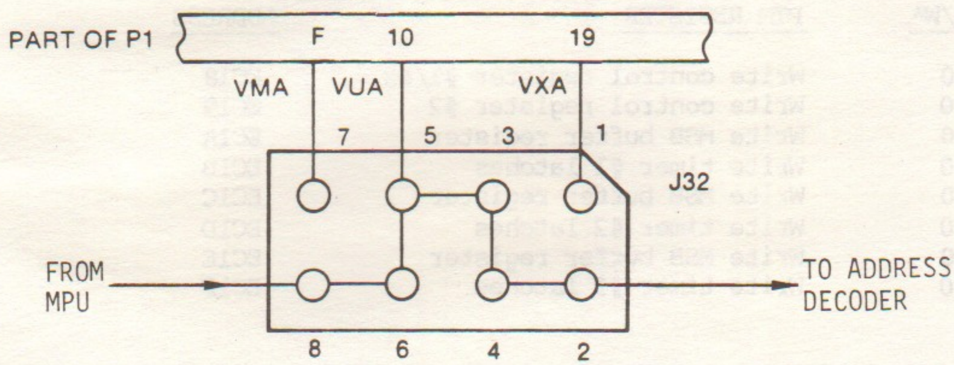


FIGURE 2-16. Memory Map Selection and Bus Mode Control

2.3.16 Programming the Peripheral Interface Adapter (PIA)

The PIA is assigned addresses EC10 through EC13 (see Figure 2-1) with individual PIA memory location addresses assigned as follows:

PIA REGISTER	ADDRESS
Data direction register A	EC10
Peripheral register A	EC10
Control register A	EC11
Data direction register B	EC12
Peripheral register B	EC12
Control register B	EC13

The MPU addresses the PIA as if it were memory. Therefore, all commands to the PIA are executed by the MPU as memory reference instructions. Note that bit 2 of the PIA control register is used to specify either the PIA peripheral register or the data direction register. The proper state of the CRA2 or CRB2 bit must be loaded into the corresponding PIA control register before addressing its peripheral interface or data direction register. For additional PIA programming information and considerations, refer to the MC6821 data sheet.

2.3.17 Programming the ACIA's

The MC6850 ACIA's are assigned addresses EC14 and EC15 (for serial port 1 on J1, ACIA = U11) and EC54 and EC55 (for serial port 2 on J2, ACIA = U12). Address EC14 (or EC54 for the other port) selects the ACIA control/status registers, and address EC15 (or EC55 for the other port) selects transmit/receive data registers. Refer to MC6850 data sheet for detailed programming instructions.

The MPU addresses the ACIA as if it were memory. Therefore, all commands to the ACIA are executed by the MPU as memory reference instructions. Note that the transmit/receive clock mode must be set to "divide-by-sixteen" by setting control register bits CR0 to a "one" and CR1 to a "zero".

2.3.18 Programming the PTM

The MC6840 PTM consists of three programmable timers and is assigned addresses EC18 through EC1F (see Figure 2-1). PTM memory location addresses are assigned as follows:

R/W*	PTM REGISTER	ADDRESS
0	Write control register #1/#3	EC18
0	Write control register #2	EC19
0	Write MSB buffer register	EC1A
0	Write timer #1 latches	EC1B
0	Write MSB buffer register	EC1C
0	Write timer #2 latches	EC1D
0	Write MSB buffer register	EC1E
0	Write timer #3 latches	EC1F

R/W*	PTM REGISTER	ADDRESS
1	(no op.)	EC18
1	Read status register	EC19
1	Read timer #1 counter	EC1A
1	Read LSB buffer register	EC1B
1	Read timer #2 counter	EC1C
1	Read LSB buffer register	EC1D
1	Read timer #3 counter	EC1E
1	Read LSB buffer register	EC1F

The MPU addresses the PTM as if it were memory. The MC6840 data sheet illustrates the PTM addressing and the operation of the three timers.

2.3.19 Interrupts and Interrupt Priorities

Micromodule 17 has eight potential sources of generating an IRQ* input to the MPU — two from the PIA, one from each ACIA, three from the PTM, and one from an available user input on the control bus. There are also eight potential sources of FIRQ* — two from the PIA, one from each ACIA, three from the PTM, and a user input on the control bus. Finally, there are four possible sources of NMI* — three from the PTM, and a user input on the control bus. Then, if the appropriate interrupt mask bit in the MPU condition code register is not set, the MPU reads the vector address of the user IRQ* routine at memory addresses FFF8 and FFF9, or the vector address of the user FIRQ* routine at memory addresses FFF6 and FFF7. At any time, the MPU may read the vector address of NMI* at memory addresses FFFC and FFFD.

If you are using more than one peripheral device capable of interrupting the MPU, you must prepare a software interrupt polling routine to interrogate each of these devices and determine the device initiating the interrupt. This polling routine, on determining the IRQ* or FIRQ* initiated device, causes the MPU to vector to the appropriate service routine.

In preparing the interrogation routine, you must assign priorities to the devices by assigning each device a position in the interrogation polling routine. The device interrogated first has the highest priority; the device interrogated last has the lowest priority. The PIA, an ACIA, or the PTM provides flag bits for interrogation. In the case of an external interrupt, this must be provided for by the hardware causing the external interrupt.

2.4 INSTALLATION INSTRUCTIONS

Because Micromodule 17 is intended for user-designed, microcomputer-based systems, no special installation instructions are provided. However, before installing the module into the user system or into the M6809 EXORciser, remove all power from the system and install the desired EPROM, PROM, ROM, or RAM devices into the appropriate sockets. Connect the ±12 Vdc power to the appropriate pins on the user bus for the RS-232C serial interface. The ±12 Vdc is also required if the user is going to use Micromodule 11 in conjunction with Micromodule 17 to implement the serial TTY 20-mA current loop.

2.4.1 Adapter Cable

An adapter cable is necessary to connect serial interface connector J1 or J2 to an RS-232C device. See Appendix A for construction details for such a cable, or purchase a three-foot long cable: M68RS232F with a female DB-25 connector, or M68RS232M with a male DB-25 connector. The female connector mates with a terminal cable; the male connector mates directly with the terminal.

CHAPTER 3

OPERATING INSTRUCTIONS

3.1 INTRODUCTION

This chapter gives the controls and indicators, operating procedures, and operating restrictions peculiar to Micromodule 17. For general information on the operation of MC6809 systems, refer to the M6809 EXORciser or M6809 EXORterm user's guides.

3.2 CONTROLS AND INDICATORS

There are no indicators on MM17. The only control is the pushbutton switch S1 at the upper left corner of the board. This switch is used for a local restart function and generates a system RESET signal when pressed.

3.3 OPERATING PROCEDURES

If all the jumper options and address assignments given in Chapter 2 have been chosen, and the EPROM's, PROM's, ROM's, and/or RAM's have been installed as desired, Micromodule 17 is ready to use. Turn off system power and install MM17 in a Micromodule chassis or M6809 EXORciser chassis. Connect interface cable(s) to the serial port(s) at J1 and/or J2 and/or the parallel port at J4, as required. Connect a cable to the timer port at J3 if the timer signals are needed elsewhere in the system. Turn on system power. If the system does not immediately operate, press the system RESTART button (if available) or the reset switch S1 on Micromodule 17.

3.4 OPERATING RESTRICTIONS

The MM17 board is bus-compatible with the EXORciser and the Micromodule chassis. It will work with most EXORciser and Micromodule boards, with the following exceptions:

a. MM17 will not work properly with an MC6800-, MC6802-, or MC6805-type DEbug Module (such as EXORciser DEbug I and DEbug II Modules).

b. MM17 will work with the full facilities of M6809 DEbug Module.

c. MM17 will not work with Micromodule 12, but will work with Micromodules 12-1 and 12-2, because their firmware and software are MC6809-based.

d. Dual map capability requires that all peripherals and memories must be able to be assigned to the proper map (by VUA or VXA). All EXORciser I modules will automatically respond to VUA when operating with MM17. To assign these modules to VXA, the user must modify the individual modules by cutting and jumpering a single connection at the edge connector of the EXORciser I module. The modification is the same for all EXORciser I modules, and is illustrated in Figure 3-1. Cut the incoming VUA track from pin 10 near the edge connector finger. Connect a jumper wire from the VXA signal track (pin 19) to the circuitry side of the cut track just performed. (See also Chapter 2 instructions for configuring J32 on MM17.)

e. The early 8K dynamic RAM module (MEX6815-1) requires some precaution before use with MM17. This module transfers data asynchronously. The 8K dynamic RAM module (MEX6815-1) may be used with MM17 if the following precautions are taken.

   Only a few early versions of the 8K dynamic RAM modules (MEX6815-1) used a 60-microsecond refresh cycle. This was changed to 30 microseconds. If any difficulty is encountered using MEX6815-1 8K memories with newer memories, a quick check of the refresh time should be made. The 60-microsecond timing cannot be used with newer modules.

   When using MEX6815-1 8K modules with other dynamic RAM's (including series II RAM modules), the MEX6815-1 8K module must be assigned as the master in the system.

f. The early 16K dynamic RAM module (MEX6816-1) and the EROM/RAM Module (MEX68RR) require modification before use in an M6809 EXORciser. These modules generate an Activate ($\overline{\text{ACT}}$) signal on pin 23. This signal has been redefined in MM17 as Bus Status (BS). It is necessary to disable one of these signals in order to avoid damage to either module. The recommended modification is to disable the $\overline{\text{ACT}}$ signal on the 16K dynamic RAM module or EROM/RAM module because it is not used on any other M6800 or M6809 module. Refer to Figure 3-2. To disable the $\overline{\text{ACT}}$ signal, cut the $\overline{\text{ACT}}$ signal track (pin 23) above the finger on the module edge connector, as illustrated.

g. The M6800 System Analyzer I or II can work with MM17 if the M6809 PROM's are installed and the M6809 system analyzer intercept module is used.

h. EXORdisk I can work with MM17 as long as slow memories are not installed. Using slow memories with EXORdisk I will cause read/write errors. In addition, the M6800 PROM's on the floppy disk controller module must be replaced with M6809 PROM's.

   When working with EXORdisk II or III, it is necessary to replace the M6800 PROM's with M6809 PROM's on the floppy disk controller module. A low on the Memory Not Ready (MNRDY*) line will cause the system clocks to be stretched. For this reason, it is necessary for the disk drivers to operate off the 1-MHz controller clock if the drivers are to function properly when slow memories are installed in the system.

i. The combination of Micromodule 17 with one or more MEX6815-3 dynamic RAM modules may not work properly if any of these modules is on an extender board.

j. If Micromodule 17 is with a system using MDOS, the maximum amount of off-board memory a user may have is 52K -- from $0000 to $CFFF.

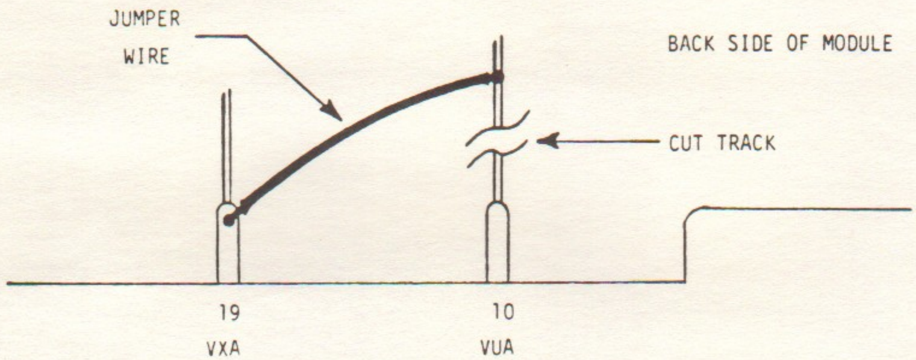


FIGURE 3-1. Assigning EXORciser I Modules to VXA

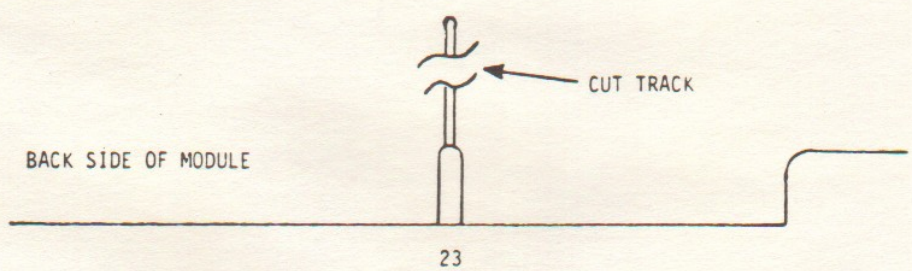


FIGURE 3-2. Modification for 16K Dynamic RAM Module (MEX6816-1) or EROM/RAM Module (MEX68RR)

CHAPTER 4

FUNCTIONAL DESCRIPTION

4.1 INTRODUCTION

This chapter provides a block diagram level description of Micromodule 17. The block diagram of MM17 is given in Figure 4-1. Refer to the MC6809 data sheet for details of MC6809 operation, and to the schematic diagram in Chapter 5 for circuit details of MM17.

4.2 MODULE DESCRIPTION

4.2.1 General

See Figure 4-1. Micromodule 17 is designed with full buffering of all address, data, and control output signals on the board, thus creating a two-section structure. The first functional section is the MPU section. This includes the address and data bus buffers, as well as the control circuitry for reset, refresh request, and bus request support. The second functional section is the peripheral section. This includes a full set of address and data bus buffers, the address decoding for all peripherals and memory, five EPROM/ROM/RAM sockets, the ACIA's, PIA, and PTM, as well as their associated interface.

4.2.2 Detailed

See the schematic diagram in Chapter 5, as well as the general timing diagram for MM17 during read and write cycles (Figure 4-2) and timing for the request and grant signals between MM17 and the bus (Figure 4-3).

An MC1455 timing device, operated as a monostable multivibrator (one-shot) functions as a restart circuit that generates a low-level RESET* signal (approximately 500 ms duration) after power is initially applied to MM17. A valid RESET* signal (one whose duration is more than 8 MPU clock periods) causes the MPU to begin to execute an initialization routine. The RESET* signal also clears all registers in the PIA to logic zero (low) so that the PIA may be configured during system initialization. The RESET* signal also pre-sets the PTM latches and counters to their maximal count values, disables the counter clocks, clears the status register interrupt flags, and sets the control register internal reset bit which holds all timers in their pre-set state. Alternatively, an external RESET* command may be applied to MM17 via connector P1. In addition to the RESET* one-shot, MM17 also provides a debounced switch to provide a system reset function.

A 4-MHz crystal provides the clock input to the MC6809 MPU. The MPU provides a divide-by-four circuit which generates the required two-phase clocks E and Q for the rest of the system.

The M6809 EXORciser/Micromodule bus signals of REFREQ* and BUSREQ* are interfaced into the BREQ* input of the MC6809 MPU. These request input lines to MM17 are sampled on the rising edge of E at U38, and must be active 50 ns prior to this edge. If either request is active, the MPU BREQ* is activated. Then, based on priority (REFREQ* has the highest priority) and present bus cycle BA and BS status, a grant (REFGNT or BUSGNT) is determined for the next bus cycle.

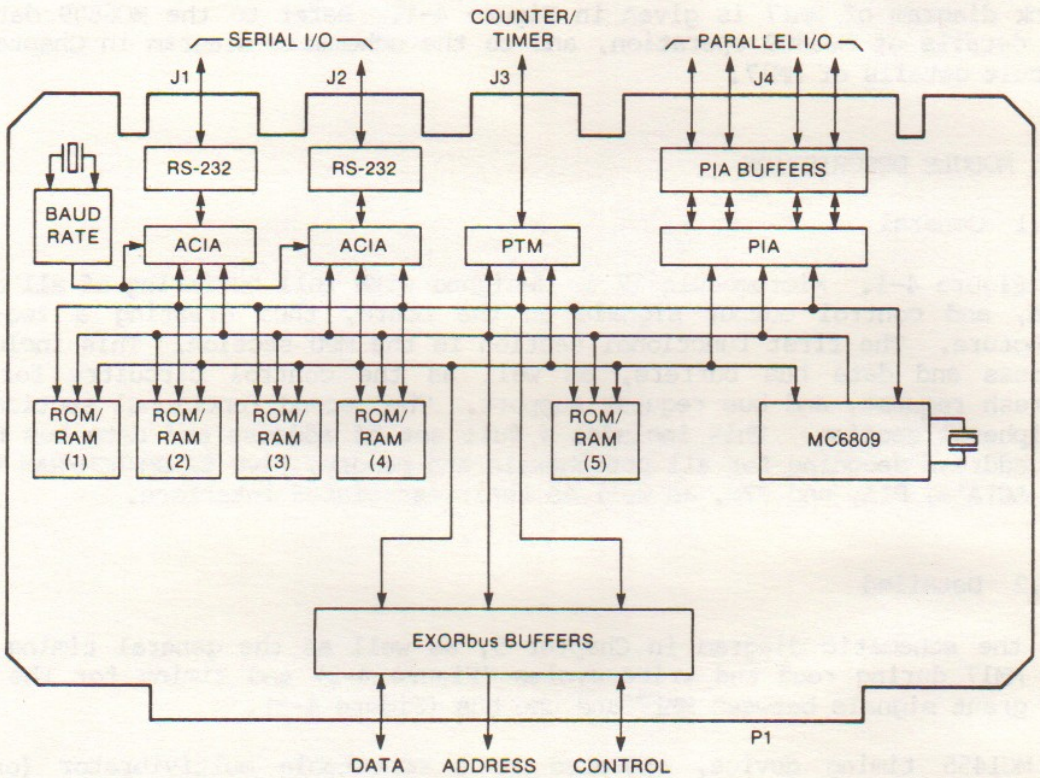


FIGURE 4-1. Micromodule 17 Block Diagram

The availability of the next bus cycle (the MPU being inactive) is based on two facts:

a. The MC6809 MPU will always relinquish the bus the cycle after its BUSREQ* input goes active.

b. It takes one cycle for the MPU to get off the bus (go inactive) and one cycle for it to get on (go active).

Therefore, BUSGNT will be issued upon the falling edge of E, and the bus will be available immediately afterward. This is possible because the MPU is in its high-impedance state during its active/inactive transitions and buffered from the EXORciser bus. This same bus request circuitry includes consideration for the self-refresh function of the MC6809, in which after 14 cycles of constant BUSREQ*, the MPU will regain the bus (bring BA low) and execute an instruction cycle. It is implemented on MM17 with U19 and U33, and is gated on the falling edge of E.

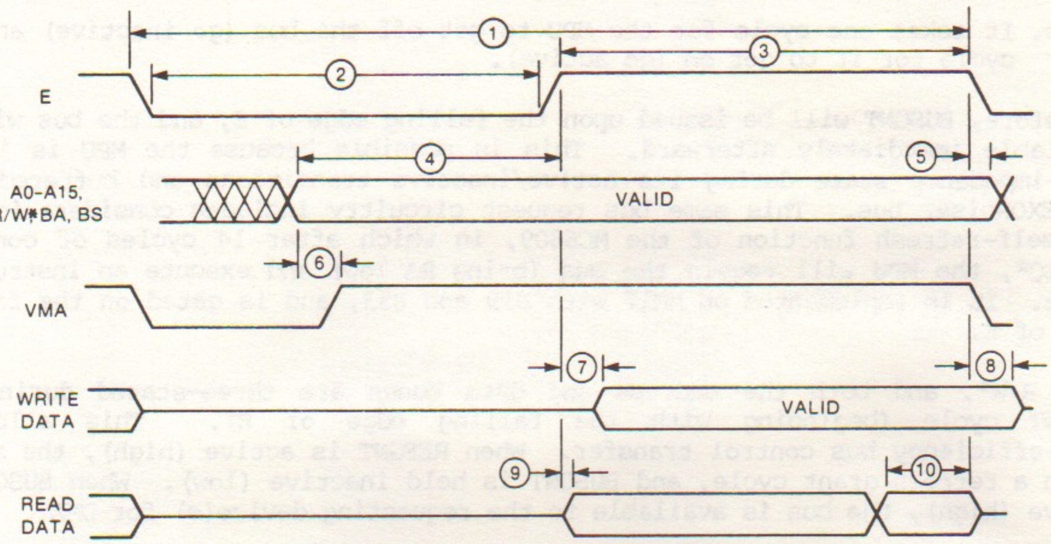
VMA, R/W*, and both the address and data buses are three-stated during the BUSGNT cycle (beginning with the falling edge of E). This allows a high-efficiency bus control transfer. When REFGNT is active (high), the system is in a refresh grant cycle, and BUSGNT is held inactive (low). When BUSGNT is active (high), the bus is available to the requesting device(s) for DMA.

The MM17 data bus is used to perform data transfers between the MPU and various devices (PROM/ROM, RAM, ACIA's, PIA, PTM). For greater memory and I/O capacity, additional devices can be added external to the Monoboard. However, all data transfers between MM17 and the external devices must be made via the data bus interface. A bus enable circuit -- composed of gates of U19, U24, U25, and U26 -- controls the data bus interface for the peripheral chips. This circuit utilizes signals BR/W, E*, and a signal from U15-9. During any on-board peripheral I/O operation, U15-9 is high if any of the peripheral chips are enabled. In addition, during an on-board read operation, BR/W is high, enabling the data bus drivers, and WR is low, disabling the data bus receivers. During an on-board write, BR/W is low, disabling the data bus drivers, and WR is high, enabling the data bus receivers.

Another bus enable circuit -- composed of gates of U19, U25, and U26 -- controls the data bus for the MPU. This circuit utilizes the on-board signals MR/W* and E* (MPU Read/Write and MPU Bus Enable). When E is low, these signals enable the data bus receivers during an MPU read operation, and enable the data bus drivers during an MPU write operation. However, the state of the BG* signal controls the enabling of the MPU data bus transceivers.

The MM17 address bus is used to select each of the memory locations within the Micromodule system. MM17 uses a fully decoded addressing scheme to uniquely address each on-board PROM/ROM, RAM, ACIA, PIA, and PTM. The memory map in Figure 2-1 shows the assignments.

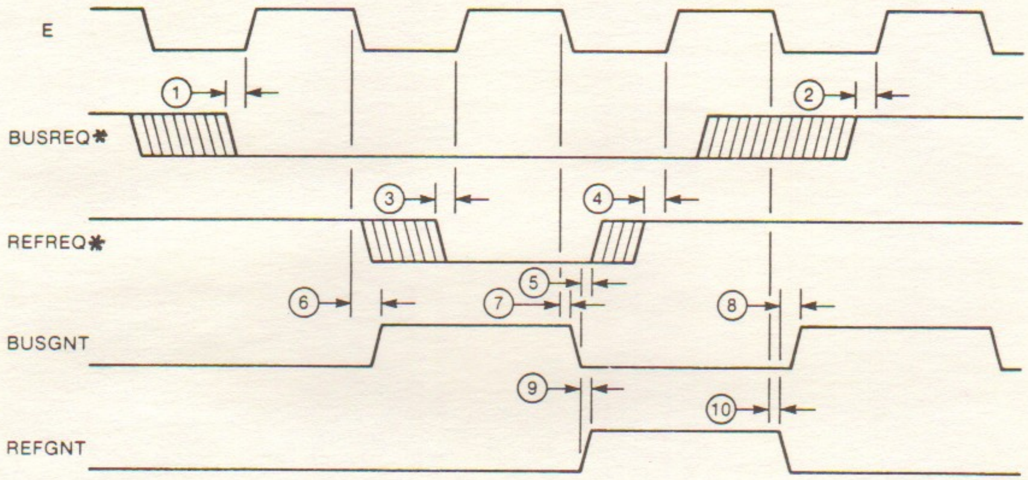
The ACIA line drivers and receivers provide two RS-232C compatible serial I/O ports. The baud rate is selected by means of jumper connections on J19 (J20) (see paragraph 2.3.7). A baud rate generator drives the Tx and Rx clock inputs of the ACIA at 16 times the baud rate(s). When clock frequencies of 16 or 64 times the bit rate are used, data and clock synchronization occurs automatically within the ACIA. During ACIA initialization, a divide-by-16 counter ratio should be loaded into the ACIA Control Register.



NUMBER	CHARACTERISTIC	TIME IN NANOSECONDS MIN.	MAX.
1	Cycle time	1000	-
2	E low time	430	-
3	E high time	450	-
4	A0-A15 valid to E high	300	-
5	A0-A15 hold time	15	-
6	A0-A15 valid to VMA high	30	-
7	E high to write data valid	-	25
8	Write data hold time	15	-
9	E high to read data low-Z	0	-
10	Read data valid to E low	100	-

NOTE: Read data access time is 590 nanoseconds maximum.

FIGURE 4-2. Micromodule 17 Read and Write Cycle Timing



NUMBER	CHARACTERISTIC	TIME IN NANOSECONDS MIN.	MAX.
1	BUSREQ* low to E high	50	-
2	BUSREQ* high to E high	55	-
3	REFREQ* low to E high	50	-
4	REFREQ* high to E high	55	-
5	REFGNT high to REFREQ* high	0	-
6	E low to BUSGNT high	-	146
7	E low to BUSGNT low	-	9
8	REFGNT low to BUSGNT high	-	36
9	BUSGNT low to REFGNT high	-	21
10	E low to REFGNT low	-	6

FIGURE 4-3. Micromodule 17 Bus and Refresh Request and Grant Timing

CHAPTER 5

SUPPORT INFORMATION

5.1 INTRODUCTION

This chapter provides the interconnect signal descriptions, parts lists, and schematic diagrams for Micromodule 17.

5.2 INTERCONNECT SIGNALS

Table 5-1 describes the signals on the M6809-EXORciser-compatible bus 86-pin edge connector P1. Table 5-2 describes the signals on the two RS-232C 20-pin serial port edge connectors J1 and J2. Table 5-3 describes the signals on the 20-pin timer edge connector J3, and Table 5-4 describes the signals on the 50-pin parallel port edge connector J4.

TABLE 5-1. Connector P1 Bus Interface Signals

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
A,B,C	+5 VDC	+5 Vdc POWER - Used by the module logic circuits.
D	BIRQ*	INTERRUPT REQUEST - An active low, level-sensitive, wired-OR, input signal requests the generation of an interrupt sequence by the on-board MC6809 MPU. This signal is latched by the MPU on the leading edge of E, but will not be recognized by the MPU until it completes execution of the present instruction. At that time, if the interrupt mask bit in the MPU condition code register is not set, the MPU will start executing the interrupt sequence.
E	NMI*	NONMASKABLE INTERRUPT - An active low, edge-sensitive, wired-OR, input signal requests the generation of a nonmaskable interrupt sequence by the on-board MC6809 MPU. This signal is sampled on the leading edge of E, and must have been inactive for one cycle for recognition by the MPU. This occurs following the completed execution of the present instruction. At that time, regardless of the state of the interrupt mask bit in the MPU condition code register, the MPU will begin executing the non-maskable interrupt sequence.
F	VMA	VALID MEMORY ADDRESS - An active high output signal generated by the MM17 circuitry to indicate the presence of a valid memory address on the bus. This signal is jumper selectable and is used in conjunction with an M6809 DEbug Module; otherwise, the jumper is made to VUA (pin 10). This line will be in a high-impedance state while BUSGNT is active.

TABLE 5-1. Connector P1 Bus Interface Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
H		Not used.
J	E	E - An active high, bi-phase clock, output signal generated by the MC6809 MPU. In association with the other bi-phase clock signal, Q, it indicates transitions in the MC6809 MPU cycle. This signal is extended in quarter-cycle increments through the use of the MNRDY* signal and, thus, should not be used as a real-time clock base.
K		Not used.
L	MEMCLK	MEMORY CLOCK - An active high clock output signal. This signal, in phase with E, is used as a clock by all system memory modules. This signal is extended in quarter-cycle increments through the use of the MNRDY* signal and, thus, should not be used as a real-time clock base.
M	-12 VDC	-12 Vdc Power - Used by serial interface circuitry.
N	BUSREQ*	BUS REQUEST - An active low, wired-OR, input signal requests the MM17 circuitry to establish an M6809 bus request. The request, which must be active 40 nsec prior to the leading edge of E, is acknowledged through the BUSGNT signal (pin 15). This signal is the only means of gaining access to the system bus. Refer to the BUSGNT description (pin 15) for further details.
P	BA	BUS AVAILABLE - An active high output signal which indicates the status of the on-board MC6809 MPU, but does not reflect the status of the system bus (this is done through BUSGNT - pin 15). The signal is useful, in conjunction with BS (pin 23), in detecting MPU halt, interrupt, and sync acknowledge states. BA BS MPU STATE 0 0 Normal (running) 0 1 Interrupt acknowledge 1 0 Sync acknowledge 1 1 Halt or bus grant
R	MNRDY*	MEMORY NOT READY - An active low, wired-OR, input signal which, when active during the last quarter of the MPU cycle (E active, Q inactive), extends E high and Q low in quarter-cycle increments. It will also extend MEMCLK (pin L) and CLOCK (pin 18). This line may be held active for no longer than 10 microseconds. This signal permits the system to work with slow memory modules.

TABLE 5-1. Connector P1 Bus Interface Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
S		Not used.
T	+12 VDC	+12 Vdc POWER - Used by serial interface circuitry.
U,V,W		Not used.
X,Y,Z	GND	GROUND
$\overline{A}$	BFIRQ*	FAST INTERRUPT REQUEST - An active low, level-sensitive, wired-OR, input signal requests the generation of a fast interrupt sequence by the on-board MC6809 MPU. This signal is latched by the MPU on the leading edge of E, but will not be recognized by the MPU until it completes execution of the present instruction. At that time, if the interrupt mask bit in the MPU condition code register is not set, the MPU will start executing the fast interrupt sequence. This sequence is fast in the sense that it only stacks the return address and condition codes.
$\overline{B}$-$\overline{F}$		Not used.
$\overline{H}$	D3*	DATA bus (bit 3) - One of eight bidirectional data lines used to provide a two-way data transfer between MM17 and all other plug-in modules within the system. The data bus drivers on the other modules are in their off or high impedance state except when selected during a valid memory read operation. The data bus drivers of MM17 are in a high-impedance state while BUSGNT (pin 15) is active.
$\overline{J}$	D7*	DATA bus (bit 7) - Same as D3* on pin $\overline{H}$.
$\overline{K}$	D2*	DATA bus (bit 2) - Same as D3* on pin $\overline{H}$.
$\overline{L}$	D6*	DATA bus (bit 6) - Same as D3* on pin $\overline{H}$.
$\overline{M}$	A14	ADDRESS bus (bit 14) - One of 16 address lines output by Micromodule 17 that permits the MPU to select any addressable memory location within the system. The address bus drivers of MM17 are in a high-impedance state while BUSGNT (pin 15) is active.
$\overline{N}$	A13	ADDRESS bus (bit 13) - Same as A14 on pin $\overline{M}$.
$\overline{P}$	A10	ADDRESS bus (bit 10) - Same as A14 on pin $\overline{M}$.
$\overline{R}$	A9	ADDRESS bus (bit 9) - Same as A14 on pin $\overline{M}$.
$\overline{S}$	A6	ADDRESS bus (bit 6) - Same as A14 on pin $\overline{M}$.

TABLE 5-1. Connector P1 Bus Interface Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
$\overline{T}$	A5	ADDRESS bus (bit 5) - Same as A14 on pin $\overline{M}$.
$\overline{U}$	A2	ADDRESS bus (bit 2) - Same as A14 on pin $\overline{M}$.
$\overline{V}$	A1	ADDRESS bus (bit 1) - Same as A14 on pin $\overline{M}$.
$\overline{W}$,$\overline{X}$,$\overline{Y}$	GND	GROUND
1-3	+5 VDC	+5 Vdc power - Used by the module logic circuits.
4	HALT*	HALT - An active low, wired-OR, input signal requests the halting of the on-board MC6809 MPU. This signal is latched by the MPU on the leading edge of E, and the MPU will halt following the completion of the present instruction. The halt condition, indicated through BA (pin P) and BS (pin 23), does not grant access to the system bus. Refer to BUSREQ* and BUSGNT.
5	RESET*	RESET - An active low, wired-OR, input/output signal which, when active, resets the MC6809 MPU, as well as other peripheral devices and system modules. The MM17 circuitry holds the signal active for approximately 0.5 seconds following power-up or while the on-board reset switch is depressed.
6	R/W*	READ/WRITE - An active low (write operation) output signal generated by the MC6809 MPU, which indicates to other modules in the system what action the MPU is taking and what is the direction of the data bus.
7	Q	QUADRATURE CLOCK - An active high, bi-phase clock, output signal generated by the MC6809 MPU. In association with the other bi-phase clock, E, it indicates transitions in the MC6809 MPU cycle. Q is extended in its low state in response to MNRDY* low.
8,9		Not used.
10	VUA	VALID USER ADDRESS - An active high output signal generated by the MM17 circuitry to indicate the presence of a valid user address on the bus. This signal is jumper selectable and is used when an M6809 DEbug Module is not present; otherwise, the jumper is made to VMA. This line will be in a high-impedance state while BUSGNT is active. On-board memory and I/O may be placed in the user memory map through strap selection.
11	-12 VDC	-12 Vdc power - Used by serial interface circuitry.

TABLE 5-1. Connector P1 Bus Interface Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
12	REFREQ*	REFRESH REQUEST - An active low, wired-OR, input signal requests a bus cycle for the refresh of dynamic memory modules. A refresh cycle disables the MPU for two cycles. Refer to REFGNT (pin 13) for further information.
13	REFGNT	REFRESH GRANT - An active high output signal which acknowledges the request for a refresh cycle and indicates the refresh grant cycle. While REFGNT is active, BUSGNT is held inactive. MPU is inactive during REFGNT, as well as the following bus cycle, making refresh a two-cycle operation.
14		Not used.
15	BUSGNT	BUS GRANT - An active high output signal generated by the MM17 circuitry to acknowledge the request for the system bus, through BUSREQ* (pin N), and to indicate the granting of bus access. This signal tightly controls access to the system bus. The signal is inactive during the first 50 nsec of every bus cycle, forcing all bus masters (those modules which drive the address bus, VMA/VUA/VXA, R/W*, and data bus) off the bus for the first 50 nsec of every bus cycle. This avoids contention for the shared bus signals during bus mastership transfers. If this signal is inactive, MM17 is bus master. The signal is held inactive during refresh grant cycles and during MC6809 MPU internal refresh cycles.
16	+12 VDC	+12 Vdc power - Used by serial interface circuitry.
17		Not used.
18	CLK	CLOCK - An active high, symmetrical clock, output signal generated by the MM17 circuitry, which closely resembles E. This signal is extended in quarter-cycle increments through use of the MNRDY* signal and, thus, should not be used as a real-time clock base.
19	VXA	VALID EXECUTIVE ADDRESS - An active high output signal which is strap selectable as an alternative to VUA when used without an M6809 DEbug Module. On-board memory and I/O may be placed in the executive memory map through strap selection.
20-22	GND	GROUND
23	BS	BUS STATUS - An active high output signal generated by the MC6809 MPU, which, in conjunction with the BA signal (pin P), is useful for determining MPU halt, interrupt, and sync acknowledge states.

TABLE 5-1. Connector P1 Bus Interface Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
24-28		Not used.
29	D1*	DATA bus (bit 1) - Same as D3* on pin $\overline{H}$.
30	D5*	DATA bus (bit 5) - Same as D3* on pin $\overline{H}$.
31	D0*	DATA bus (bit 0) - Same as D3* on pin $\overline{H}$.
32	D4*	DATA bus (bit 4) - Same as D3* on pin $\overline{H}$.
33	A15	ADDRESS bus (bit 15) - Same as A14 on pin $\overline{M}$.
34	A12	ADDRESS bus (bit 12) - Same as A14 on pin $\overline{M}$.
35	A11	ADDRESS bus (bit 11) - Same as A14 on pin $\overline{M}$.
36	A8	ADDRESS bus (bit 8) - Same as A14 on pin $\overline{M}$.
37	A7	ADDRESS bus (bit 7) - Same as A14 on pin $\overline{M}$.
38	A4	ADDRESS bus (bit 4) - Same as A14 on pin $\overline{M}$.
39	A3	ADDRESS bus (bit 3) - Same as A14 on pin $\overline{M}$.
40	A0	ADDRESS bus (bit 0) - Same as A14 on pin $\overline{M}$.
41-43	GND	GROUND

TABLE 5-2. Connectors J1 and J2 Serial Interface Signals

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
1,4,8, 12,16,17, 18,19,20 (NOTE)		Not used.
2	+12 VDC	Strappable to +12 Vdc power.
3	TXD	TRANSMITTED DATA - The line through which the terminal sends data to the modem.
5	RXD	RECEIVED DATA - The line through which the modem sends data to the terminal.
6 (NOTE)	+5 VDC	Strappable to +5 Vdc power.
7	RTS	REQUEST TO SEND - The line through which the terminal requests permission to transmit data to the modem.
9	CTS	CLEAR TO SEND - The line through which the modem acknowledges the acceptance of a terminal request to send data.
10	-12 VDC	Strappable to -12 Vdc power.
11	DSR	DATA SET READY - The line through which the modem indicates its on-line, in-service, or active status.
13 (NOTE)	GND	GROUND
14	DTR	DATA TERMINAL READY - The line through which the terminal indicates its on-line, in-service, or active status.
15	DCD	DATA CARRIER DETECT - The line through which the modem indicates that its interfacing communications channel is in an acceptable active state.

NOTE: On some issue B boards, pins 4 and 19 are connected to ground, and pin 17 is connected to pin 6. This is not consistent with RS-232C.

TABLE 5-3. Connector J3 Timer Interface Signals

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
1	G1*	GATE INPUT 1 - Low level asynchronous TTL compatible input signal as trigger or clock gating to Timer.
3	O1	TIMER OUTPUT 1 - High level output from PTM capable of driving up to two TTL loads.
5	C1*	CLOCK INPUT 1 - Low level asynchronous TTL voltage level input signal used to decrement Timer.
7	G2*	GATE INPUT 2 - Same as J3-1.
9	O2	TIMER OUTPUT 2 - Same as J3-3.
11	C2*	CLOCK INPUT 2 - Same as J3-5.
13	G3*	GATE INPUT 3 - Same as J3-1.
15	O3	TIMER OUTPUT 3 - Same as J3-3.
17	C3*	CLOCK INPUT 3 - Same as J3-5.
All even pins plus pin 19	GND	GROUND

TABLE 5-4. Connector J4 Parallel Interface Signals

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
All even pins	GND	GROUND - Signal return line.
1,49	+5 VDC	+5 Vdc power - Strappable power for the port.
3,5,7		Not used.
9	CB2	CONTROL bit 2, side B - Buffered second control bit of the second section of the PIA. This signal may be used as either an input or an output.
11	CB1	CONTROL bit 1, side B - Buffered first control bit of the second section of the PIA. This signal is always an input to the PIA.
13	CA2	CONTROL bit 2, side A - Buffered second control bit of the first section of the PIA. This signal may be used as either an input or an output.
15	CA1	CONTROL bit 1, side A - Buffered first control bit of the first section of the PIA. This signal is always an input to the PIA.
17	IO15	INPUT/OUTPUT line 15 - Buffered data input or output line from PB7 on the PIA. A logic 0 in bit 7 of the B data direction register makes this line function as an input, while a 1 makes it function as an output.
19	IO14	INPUT/OUTPUT line 14 - Same as IO15, except from PB6 on the PIA, and controlled by bit 6 of the B data direction register.
21	IO13	INPUT/OUTPUT line 13 - Same as IO15, except from PB5 on the PIA, and controlled by bit 5 of the B data direction register.
23	IO12	INPUT/OUTPUT line 12 - Same as IO15, except from PB4 on the PIA, and controlled by bit 4 of the B data direction register.
25	IO11	INPUT/OUTPUT line 11 - Same as IO15, except from PB3 on the PIA, and controlled by bit 3 of the B data direction register.
27	IO10	INPUT/OUTPUT line 10 - Same as IO15, except from PB2 on the PIA, and controlled by bit 2 of the B data direction register.
29	IO9	INPUT/OUTPUT line 9 - Same as IO15, except from PB1 on the PIA, and controlled by bit 1 of the B data direction register.

TABLE 5-4. Connector J4 Parallel Interface Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
31	IO8	INPUT/OUTPUT line 8 - Same as IO15, except from PB0 on the PIA, and controlled by bit 0 of the B data direction register.
33	IO7	INPUT/OUTPUT line 7 - Same as IO15, except from PA7 on the PIA, and controlled by bit 7 of the A data direction register.
35	IO6	INPUT/OUTPUT line 6 - Same as IO15, except from PA6 on the PIA, and controlled by bit 6 of the A data direction register.
37	IO5	INPUT/OUTPUT line 5 - Same as IO15, except from PA5 on the PIA, and controlled by bit 5 of the A data direction register.
39	IO4	INPUT/OUTPUT line 4 - Same as IO15, except from PA4 on the PIA, and controlled by bit 4 of the A data direction register.
41	IO3	INPUT/OUTPUT line 3 - Same as IO15, except from PA3 on the PIA, and controlled by bit 3 of the A data direction register.
43	IO2	INPUT/OUTPUT line 2 - Same as IO15, except from PA2 on the PIA, and controlled by bit 2 of the A data direction register.
45	IO1	INPUT/OUTPUT line 1 - Same as IO15, except from PA1 on the PIA, and controlled by bit 1 of the A data direction register.
47	IO0	INPUT/OUTPUT line 0 - Same as IO15, except from PA0 on the PIA, and controlled by bit 0 of the A data direction register.

5.3 PARTS LISTS

Table 5-5 is the parts list for Micromodule 17. Parts locations are shown in Figure 5-1.

TABLE 5-5. Micromodule 17 Parts List

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
-	84-W8094B01	Printed Wiring Board, Micromodule 17
-	55NW9403A12	Ejector card, .062 thick, green (2 required)
C1-C6,C12, C19,C25,C26, C35	21NW9702A09	Capacitor, ceramic, 0.1 uF @ 50 Vdc
C7-C11,C13-C18, C20,C21,C27-C33	21SW992C025	Capacitor, ceramic, 0.100 uF @ 50 Vdc
C22,C23	21NW9629A09	Capacitor, mica, radial lead, 27 pF @ 500 Vdc, $\pm5\%$
C24	21NW9604A11	Capacitor, ceramic, 0.47 uF @ 50 Vdc, $\pm20\%$
C34	23NW9618A33	Capacitor, electrolytic, axial leads, 22 uF @ 25 Vac
E1,E2	-	Customer-supplied turret terminal studs for EXT CLK and GND.
J1,J2,J3	-	20-pin edge connectors on printed wiring board.
J4	-	50-pin edge connector on printed wiring board.
J5,J7,J18	-	Not used.
J6,J8-J12,J14, J16,J17,J22, J23,J28,J29, J32	-	Areas on the printed wiring board for optional customer-supplied headers and/or jumpers.
J13,J15, J25,J27,J31	28NW9802D59	Header, single row, 10-pin, (15 required - cut to size for individual headers).
J19,J20	28NW9802D57	Header, single row, 5-pin (6 required - three for each header)
J21	28NW9802B21	Header, double row post, 6-pin
J24,J26,J30, J33,J34	28NW9802C29	Header, double row straight, PCB, 4-pin
-	29NW9805B17	Jumper, two position (42 required) (Used with J13, J15, J19-J21, J24-J27, J30, J31, J33, J34)

TABLE 5-5. Micromodule 17 Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
P1	-	On the printed wiring board.
R1,R2,R5,R11, R12,R14,R15, R17	06SW-124A61	Resistor, film, 3.3k ohms, 5%, 1/4 W
R3,R4,R16,R18	06SW-124A73	Resistor, film, 10k ohms, 5%, 1/4 W
R6-R9	51NW9626A49	Resistor network, 10k ohms, 7 per package
R10	51NW9626A62	Resistor network, 3.3k ohms, 9 per package
R13	06SW-124B46	Resistor, fixed, film, 10 megohms, 5%, 1/4 W
R19,R20	51NW9626A50	Resistor network, 3.3k ohms, 7 per package
R21,R22	06SW-124B22	Resistor, film, 1.0 megohms, 5%, 1/4 W
S1	40NW9801A54	Switch, push, SPDT, momentary contact
U1, U3	51NW9615B30	I.C., MC1489AL
U2, U4	51NW9615B29	I.C., MC1488L
U5	51NW9615D81	I.C., MC6840P, PTM (Programmable Timer Module)
-	09NW9811A21	Socket, I.C., DIL, low profile, 28-pin (Used with U5)
U6-U9,U29, U35,U42,U47	51NW9615C55	I.C., 8T28
-	09NW9811A04	Socket, I.C. DIL, low profile, 16-pin (Used with U6-U9 and U16)
U10,U25	51NW9615E91	I.C., SN74LS00N
U11,U12	51NW9615B94	I.C., MC6850P, ACIA (Asynchronous Communications Interface Adapter)
U13	51NW9615G45	I.C., SN74LS126N
U14	51NW9615F10	I.C., SN74LS125AN
-	09NW9811A02	Socket, I.C., DIL, low profile, copper, 14-pin (Used with U13 and U14)
U15	51NW9615D83	I.C., SN74S133N
U16	(SEE NOTE)	I.C., programmed PROM

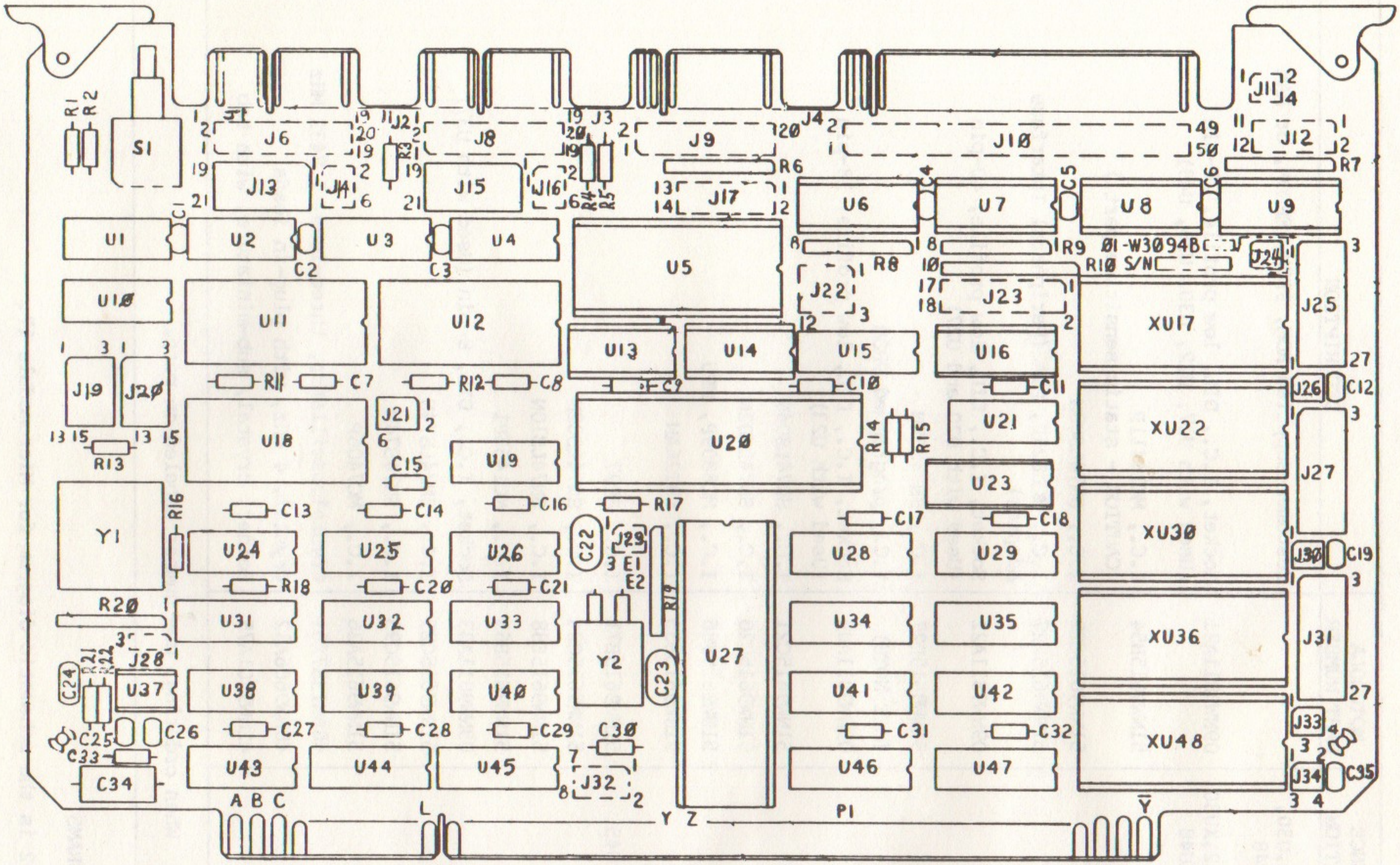
TABLE 5-5. Micromodule 17 Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
U17,U22,U30, U36,U48	-	Customer-supplied ROM, PROM, EPROM, or RAM
XU17,XU22,XU30, XU36,XU48	09NW9811A21	Socket, I.C., DIL, low profile, 28-pin (Used with U17, U22, U30, U36, U48)
U18	51NW9615B54	I.C., MC14411P (CAUTION - static sensitive part.)
U19	51NW9615C22	I.C., SN74LS08N
U20	51NW9615B27	I.C., MC6821P, PIA (Peripheral Interface Adapter)
-	09NW9811A22	Socket, I.C., DIL, low profile, 40-pin (Used with U20 and U27)
U21	51NW9615D27	I.C., SN74S32N
U23	(SEE NOTE)	I.C., programmed PROM
-	09NW9811A09	Socket, I.C., DIL, low profile, 18-pin (Used with U23)
U24,U39	51NW9615C21	I.C., SN74LS04N
U26	51NW9615C20	I.C., SN74LS02N
U27	51NW9615F86	I.C., MC6809P, MPU
U28,U34, U41,U46	51NW9615B35	I.C., N8T26AN
U31,U44,U45	51NW9615B71	I.C., 8T97
U32	51NW9615C24	I.C., SN74LS32N
U33	51NW9615E88	I.C., SN74LS10N
U37	51NW9615B65	I.C., MC1455P1
-	09NW9811A33	Socket, I.C., DIL, 8-pin (Used with U37)
U38	51NW9615C25	I.C., SN74LS74N
U40	51NW9615C95	I.C., SN74S74N
U43	51NW9615A36	I.C., MC7406P
Y1	48BW1357X01	Crystal oscillator, three-lead, 1.8432 MHz
Y2	48NW9606A32	Crystal, 4 MHz, with plug-in leads
-	42NW9401A75	Holder, crystal, sub-miniature, with tab

NOTE: When ordering, use number labeled on part.

5.4 DIAGRAMS

Figure 5-2 is the schematic diagram for Micromodule 17.



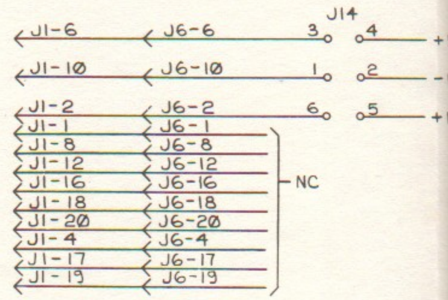
NOTE: Some issue B and issue C boards have the P1 edge connector pins U, V, W, and $\overline{F}$ labeled on the wrong pins.

FIGURE 5-1. Micromodule 17 Parts Location

NOTES:

1. FOR REFERENCE DRAWING REFER TO BILL OF MATERIAL.
2. UNLESS OTHERWISE SPECIFIED.
   ALL RESISTORS ARE IN OHMS, ± 5PCT, 1/4 WATT.
   ALL CAPACITORS ARE IN UF.
   ALL VOLTAGES ARE DC.
3. INTERRUPTED LINES CODED WITH THE SAME LETTER OR LETTER COMBINATIONS ARE ELECTRICALLY CONNECTED.
4. (△) DEVICE TYPE NUMBER IS FOR REFERENCE ONLY. THE NUMBER VARIES WITH THE MANUFACTURER.
5. SPECIAL SYMBOL USAGE:
   \# DENOTES – ACTIVE LOW SIGNAL.
6. INTERPRET DIAGRAM IN ACCORDANCE WITH AMERICAN NATIONAL STANDARDS INSTITUTE SPECIFICATIONS, CURRENT REVISION.

7 (△) PART TYPES ARE ABBREVIATED IN THE FIELD OF THE DRAWING. FOR FULL PART TYPE, REFER TO TABLE I.



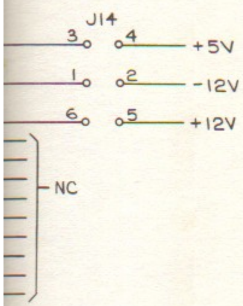
7 (△) TABLE I

REF DES	TYPE (4)	GND	+5V	-12V	+12V
U1	MC1489A	7	14		
U2	MC1488	7		1	14
U3	MC1489A	7	14		
U4	MC1488	7		1	14
U5	MC6840	1	14		
U6	8T28	8	16		
U7	8T28	8	16		
U8	8T28	8	16		
U9	8T28	8	16		
U10	74LS00	7	14		
U11	MC6850	1	12		
U12	MC6850	1	12		
U13	74LS126	7	14		
U14	74LS125	7	14		
U15	74S133	8	16		
U16	82S123	8	16		
U18	MC14411	12	24		
U19	74LS08	7	14		
U20	MC6821	1	20		
U21	74S32	7	14		
U23	82S137	9	18		
U24	74LS04	7	14		
U25	74LS00	7	14		
U26	74LS02	7	14		
U27	MC6809	1	7		
U28	8T26A	8	16		
U29	8T28	8	16		
U31	8T97	8	16		

7 (△) TABLE I CONTINUED

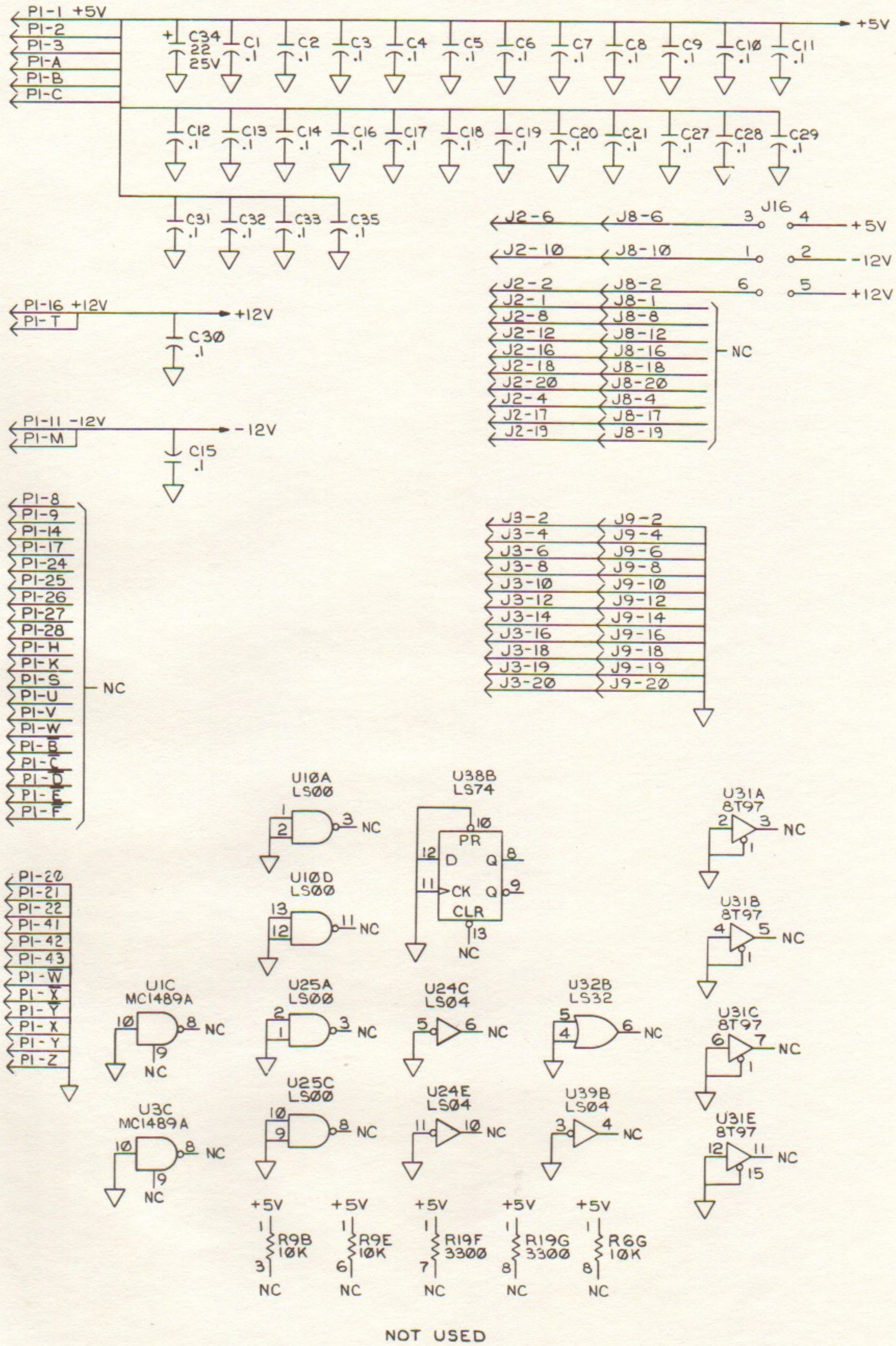
REF DES	TYPE (4)	GND	+5V	-12V
U32	74LS32	7	14	
U33	74LS10	7	14	
U34	8T26A	8	16	
U35	8T28	8	16	
U37	MC1455	1	8	
U38	74LS74	7	14	
U39	74LS04	7	14	
U40	74S74	7	14	
U41	8T26A	8	16	
U42	8T28	8	16	
U43	7406	7	14	
U44	8T97	8	16	
U45	8T97	8	16	
U46	8T26A	8	16	
U47	8T28	8	16	
XU17	(SOCKET)	14	28	
XU22	(SOCKET)	14	28	
XU30	(SOCKET)	14	28	
XU36	(SOCKET)	14	28	
XU48	(SOCKET)	14	28	
Y1	(1.8432 MHZ)	CASE		
Y2	(4.00 MHZ)	CASE		

Y2	
XU48	XU37 THRU XU47 XU31 THRU XU35 XU23 THRU XU29 XU18 THRU XU21 XU1 THRU XU16
U47	U17, 22 30, 36, 48
S1	
R22	
J34	J5, J7, J18
E2	
C35	
HIGHEST NUMBER USED	NOT USED
REFERENCE DESIGNATIONS	



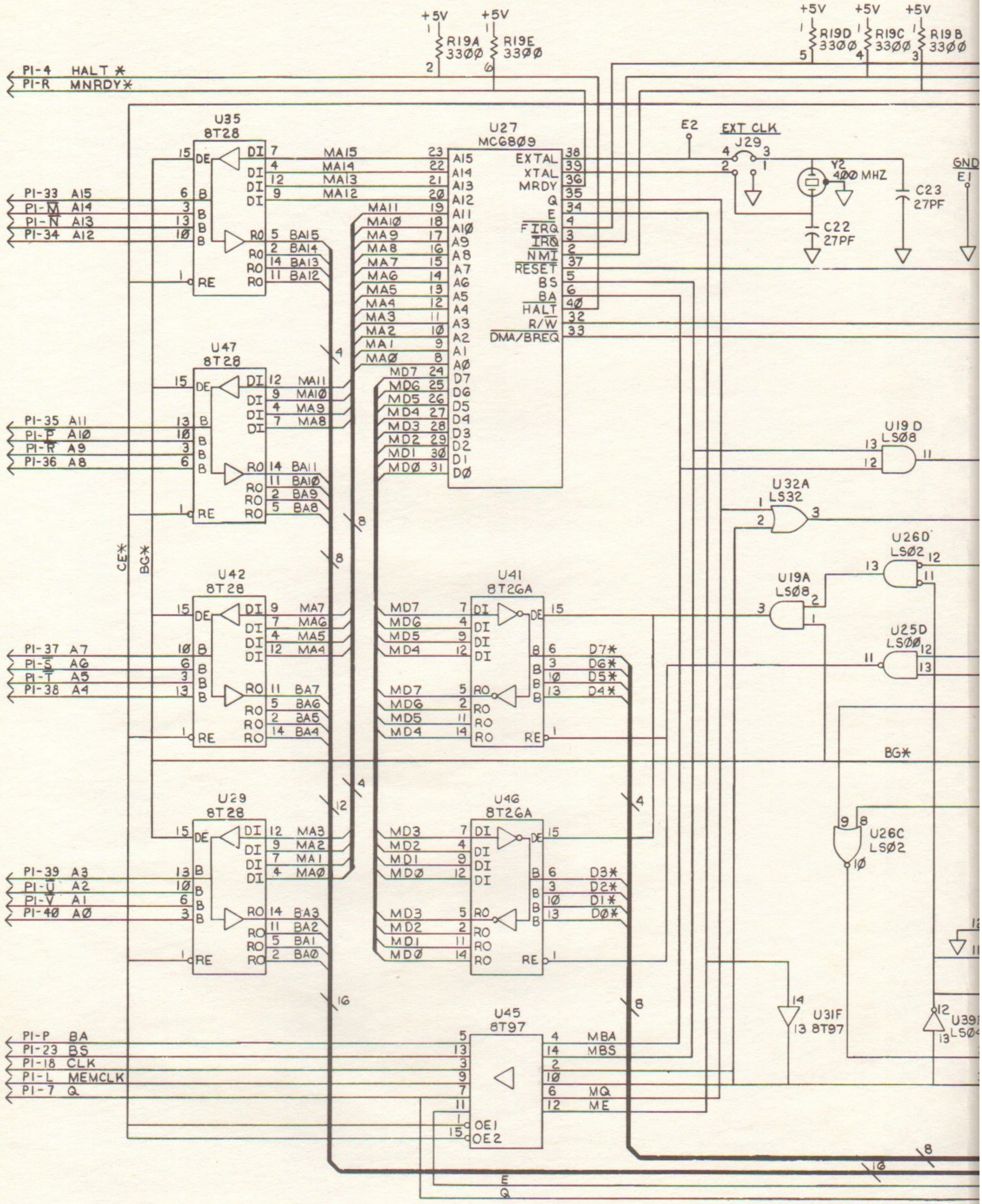
CONTINUED

GND	+5V	-12V	+12V
7	14		
7	14		
8	16		
8	16		
1	8		
7	14		
7	14		
7	14		
8	16		
8	16		
7	14		
8	16		
8	16		
8	16		
8	16		
14	28		
14	28		
14	28		
14	28		
14	28		
CASE			
CASE			



63EW3094B REV D SH1 OF 6

FIGURE 5-2. Micromodule 17 Schematic Diagram (Sheet 1 of 6)



+5V
R19A 33ØØ
R19E 33ØØ
R19D 33ØØ
R19C 33ØØ
R19B 33ØØ
P1-4 HALT*
P1-R MNRDY*
U35 8T28
U27 MC68Ø9
E2
EXT CLK
J29
Y2 4ØØ MHZ
C23 27PF
C22 27PF
GND E1
P1-33 A15
P1-M A14
P1-N A13
P1-34 A12
MA15
MA14
MA13
MA12
BA15
BA14
BA13
BA12
EXTAL
XTAL
MRDY
Q
E
FIRQ
IRQ
NMI
RESET
BS
BA
HALT
R/W
DMA/BREQ
U47 8T28
P1-35 A11
P1-P A1Ø
P1-R A9
P1-36 A8
MA11
MA1Ø
MA9
MA8
BA11
BA1Ø
BA9
BA8
MD7
MD6
MD5
MD4
MD3
MD2
MD1
MDØ
U19 D LSØ8
U32A LS32
U26D LSØ2
U19A LSØ8
U25D LSØØ
CE*
BG*
U42 8T28
P1-37 A7
P1-S A6
P1-T A5
P1-38 A4
MA7
MA6
MA5
MA4
BA7
BA6
BA5
BA4
U41 8T26A
D7*
D6*
D5*
D4*
U29 8T28
P1-39 A3
P1-U A2
P1-V A1
P1-4Ø AØ
MA3
MA2
MA1
MAØ
BA3
BA2
BA1
BAØ
U46 8T26A
D3*
D2*
D1*
DØ*
U26C LSØ2
U31F 8T97
U39 LSØ4
U45 8T97
P1-P BA
P1-23 BS
P1-18 CLK
P1-L MEMCLK
P1-7 Q
MBA
MBS
MQ
ME
OE1
OE2
E
Q

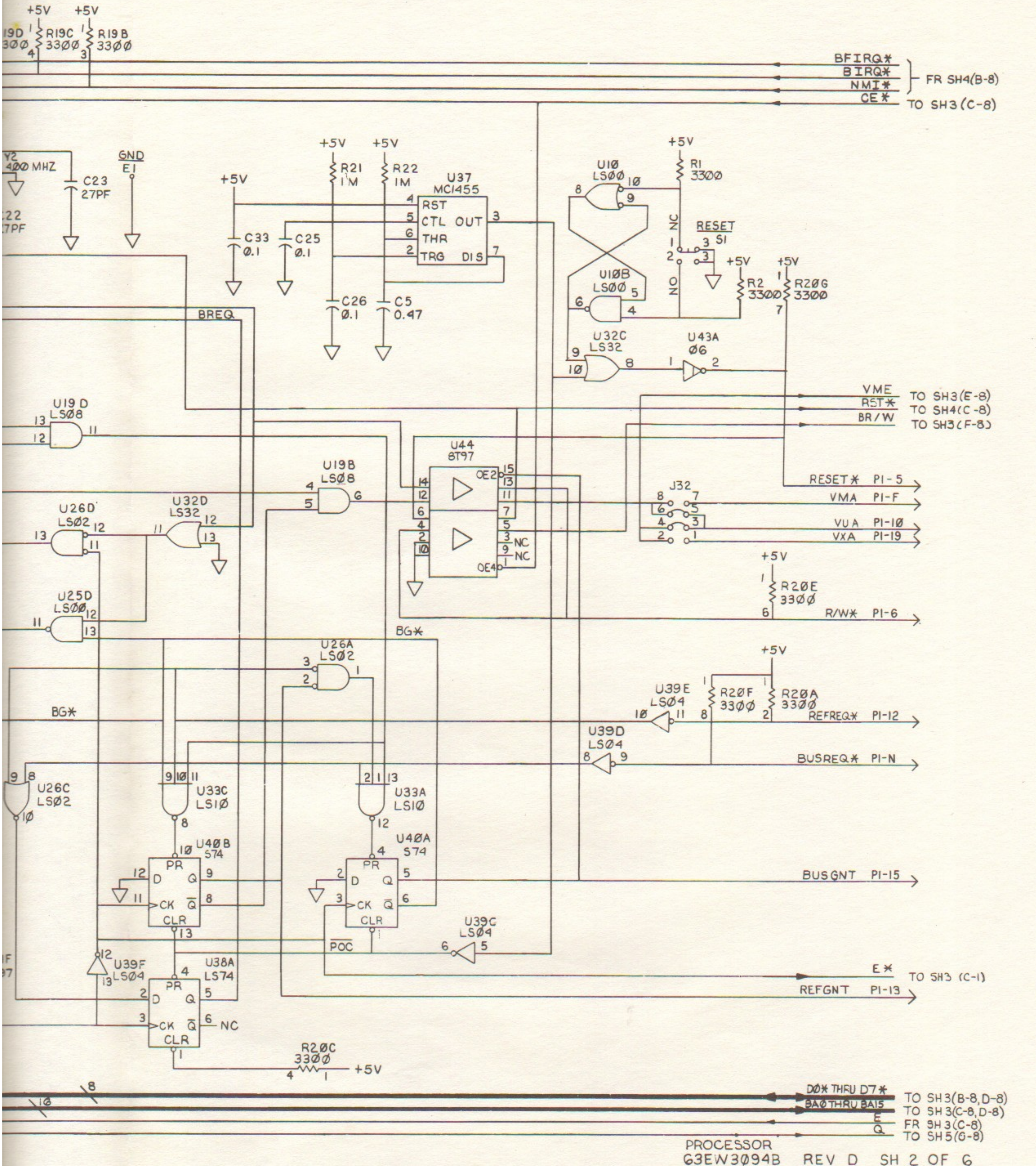
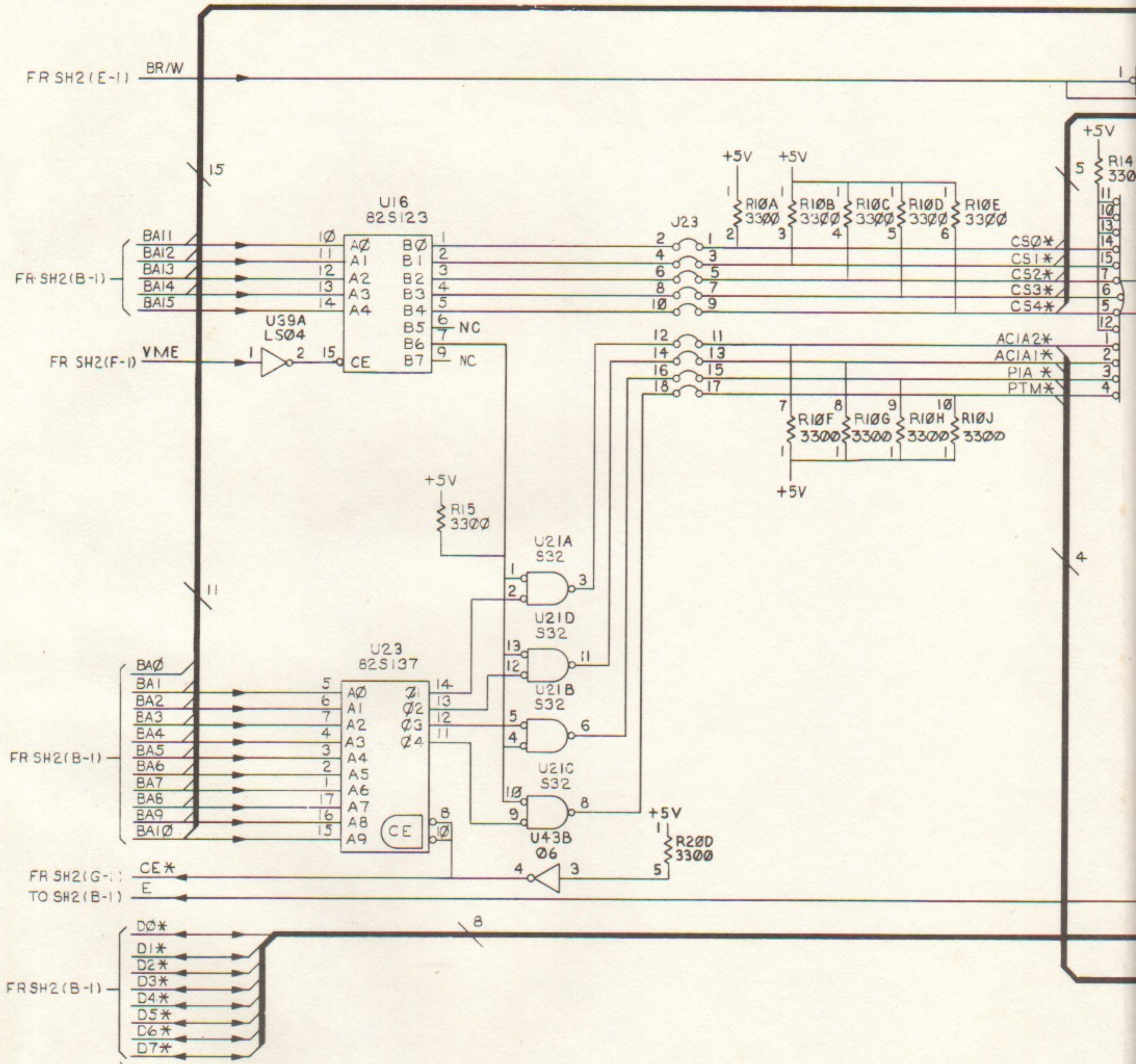
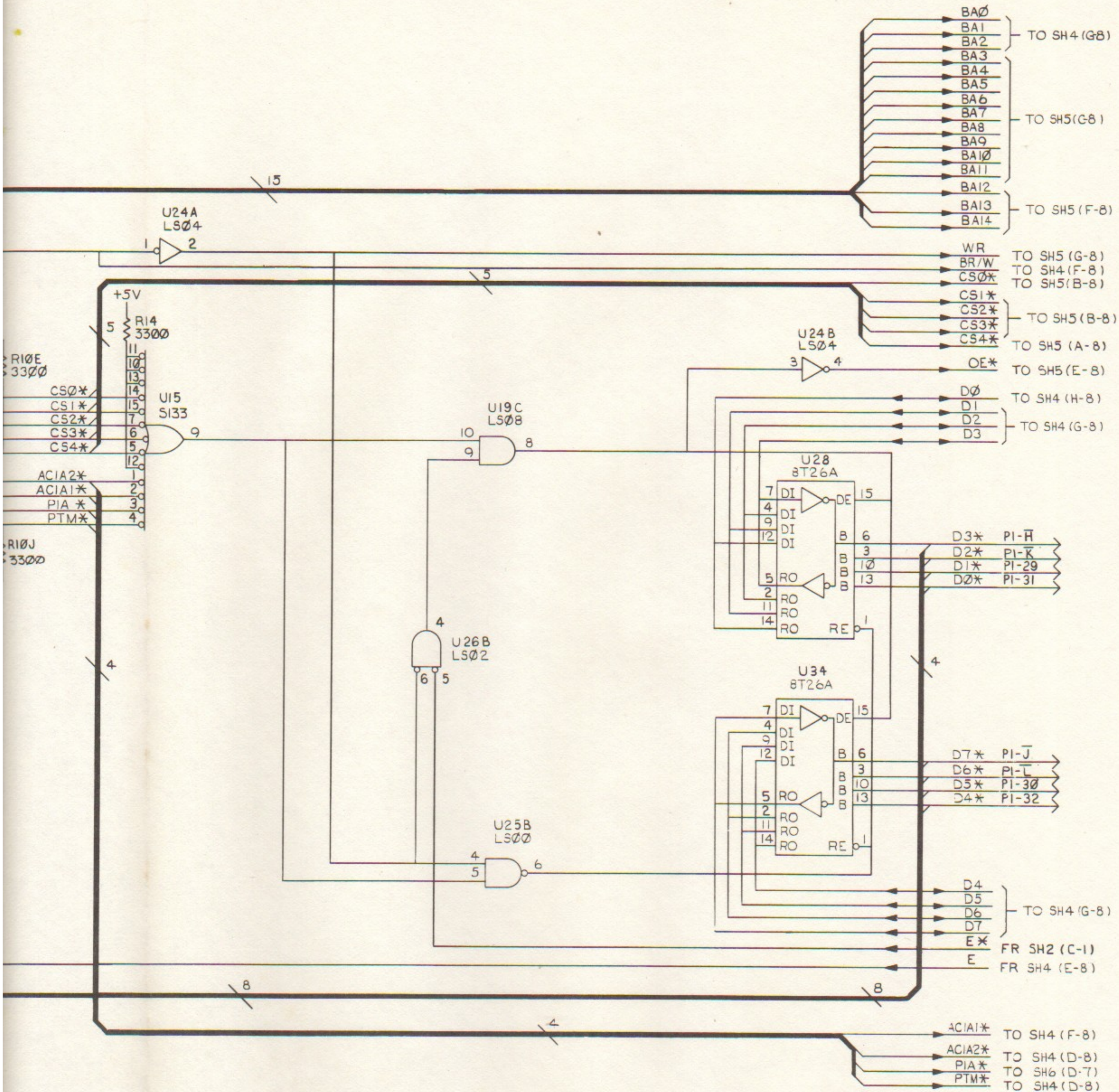


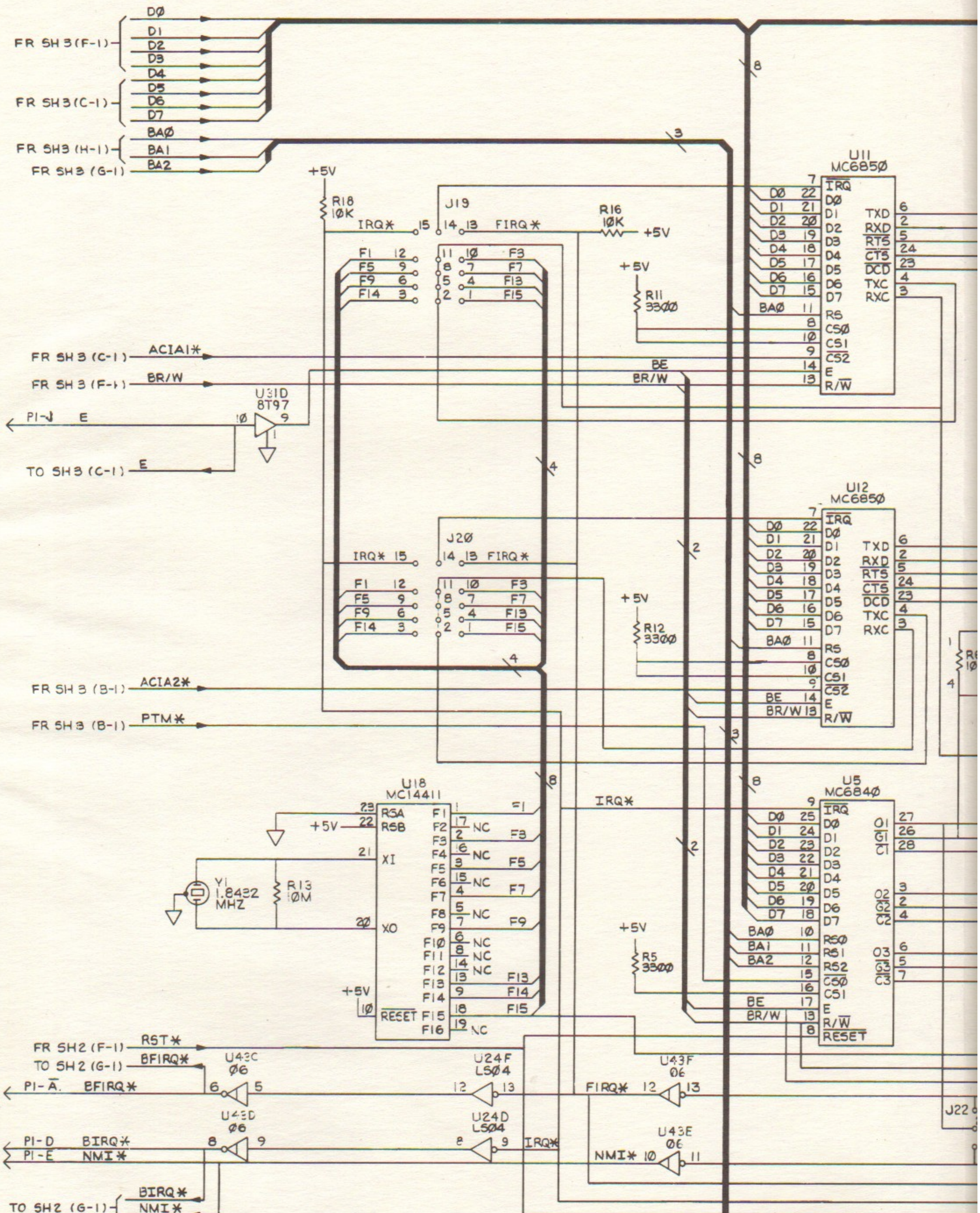
FIGURE 5-2. Micromodule 17 Schematic Diagram (Sheet 2 of 6)


FR SH2(E-1) BR/W
FR SH2(B-1) BA11 BA12 BA13 BA14 BA15
FR SH2(F-1) VME
U39A LS04
U16 82S123
A0 A1 A2 A3 A4 CE
B0 B1 B2 B3 B4 B5 B6 B7
NC
J23
+5V
R10A 3300 R10B 3300 R10C 3300 R10D 3300 R10E 3300
R10F 3300 R10G 3300 R10H 3300 R10J 3300
CS0* CS1* CS2* CS3* CS4*
ACIA2* ACIA1* PIA * PTM*
R14 330
R15 3300
U21A S32
U21D S32
U21B S32
U21C S32
U23 82S137
FR SH2(B-1) BA0 BA1 BA2 BA3 BA4 BA5 BA6 BA7 BA8 BA9 BA10
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 CE
Ø1 Ø2 Ø3 Ø4
U43B 06
R20D 3300
FR SH2(G-1) CE*
TO SH2(B-1) E
FR SH2(B-1) D0* D1* D2* D3* D4* D5* D6* D7*



MAP DECODER
63EW3Ø94B REV D SH 3 OF 6

FIGURE 5-2. Micromodule 17 Schematic Diagram (Sheet 3 of 6)


FR SH 3 (F-1)
FR SH 3 (C-1)
FR SH3 (H-1)
FR SH 3 (G-1)
DØ
D1
D2
D3
D4
D5
D6
D7
BAØ
BA1
BA2
+5V
R18
1ØK
J19
IRQ*
FIRQ*
R16
1ØK
+5V
F1
F5
F9
F14
F3
F7
F13
F15
+5V
R11
33ØØ
U11
MC685Ø
IRQ
RS
CSØ
CS1
CS2
E
R/W
TXD
RXD
RTS
CTS
DCD
TXC
RXC
ACIA1*
FR SH 3 (C-1)
BR/W
FR SH 3 (F-1)
BE
U31D
8T97
PI-J
E
TO SH 3 (C-1)
J2Ø
+5V
R12
33ØØ
U12
MC685Ø
FR SH 3 (B-1)
ACIA2*
FR SH 3 (B-1)
PTM*
U18
MC14411
RSA
RSB
XI
XO
RESET
NC
Y1
1.8432
MHZ
R13
1ØM
U5
MC684Ø
IRQ
RSØ
RS1
RS2
CSØ
CS1
E
R/W
RESET
O1
G1
C1
O2
G2
C2
O3
G3
C3
+5V
R5
33ØØ
FR SH2 (F-1)
RST*
TO SH2 (G-1)
BFIRQ*
U43C
Ø6
U24F
LSØ4
U43F
Ø6
PI-A
BFIRQ*
FIRQ*
U43D
Ø6
U24D
LSØ4
U43E
Ø6
PI-D
BIRQ*
PI-E
NMI*
IRQ*
NMI*
TO SH2 (G-1)
BIRQ*
NMI*
J22

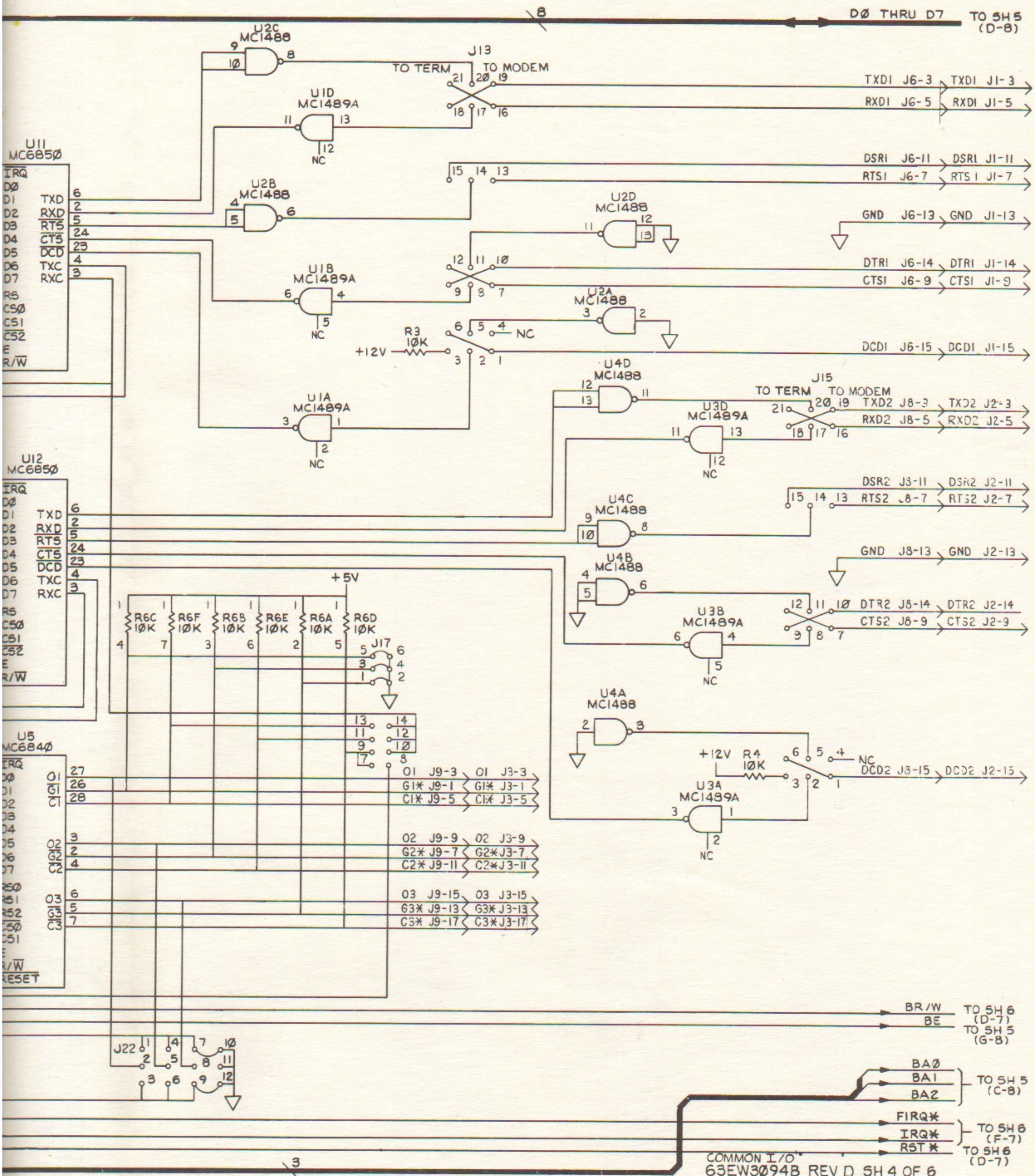
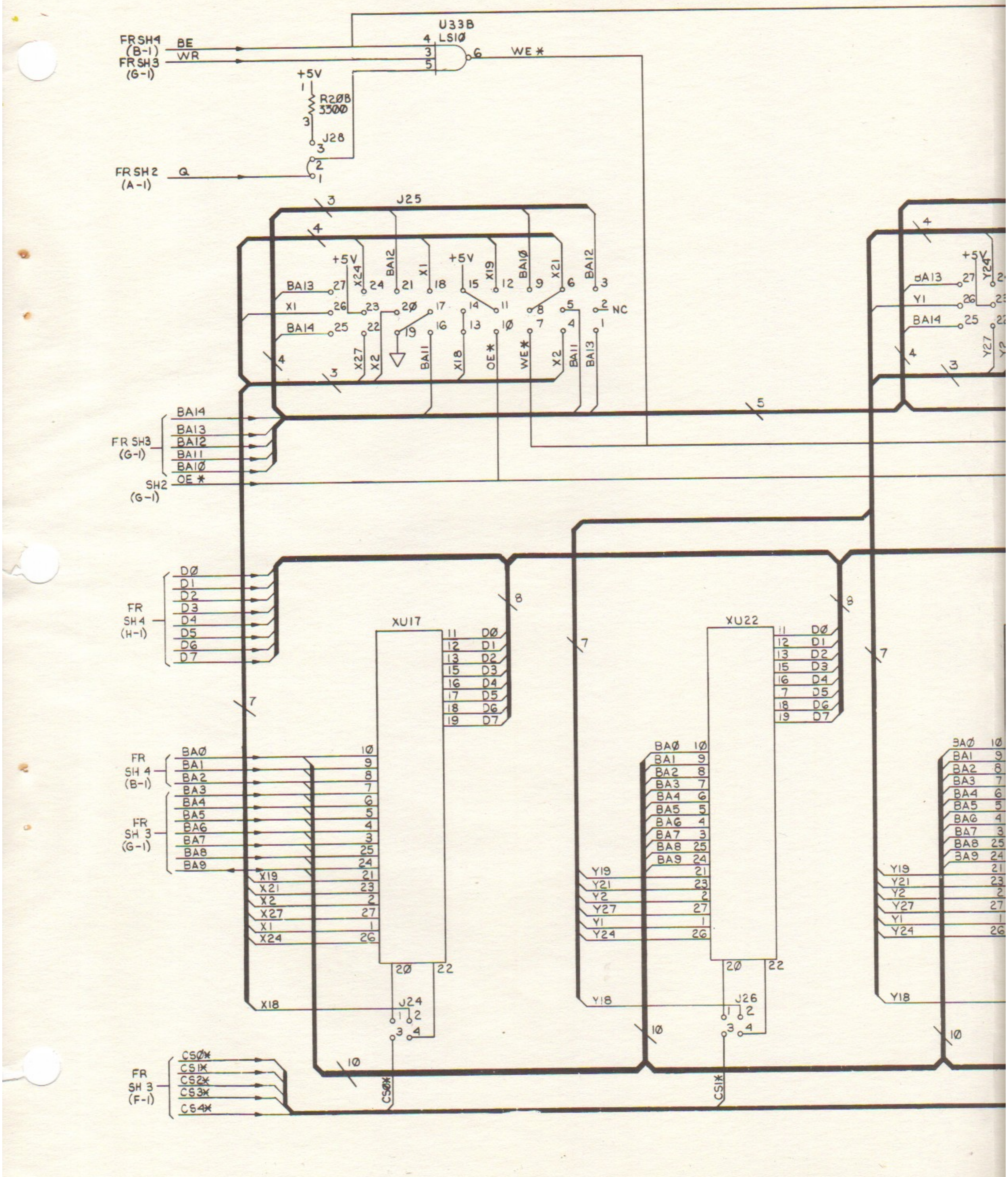


FIGURE 5-2. Micromodule 17 Schematic Diagram (Sheet 4 of 6)



U33B
LS1Ø
FR SH4 (B-1)
BE
FR SH3 (G-1)
WR
WE*
+5V
R2ØB
330Ω
J28
FR SH2 (A-1)
Q
J25
BA13
X1
BA14
X24
BA12
+5V
X19
BA1Ø
X21
NC
X27
X2
BA11
X18
OE*
WE*
BA14
BA13
BA12
BA11
BA1Ø
FR SH3 (G-1)
SH2 (G-1)
OE*
DØ
D1
D2
D3
D4
D5
D6
D7
FR SH4 (H-1)
XU17
XU22
FR SH 4 (B-1)
BAØ
BA1
BA2
FR SH 3 (G-1)
BA3
BA4
BA5
BA6
BA7
BA8
BA9
X19
X21
X2
X27
X1
X24
X18
J24
Y19
Y21
Y2
Y27
Y1
Y24
Y18
J26
FR SH 3 (F-1)
CSØ*
CS1*
CS2*
CS3*
CS4*

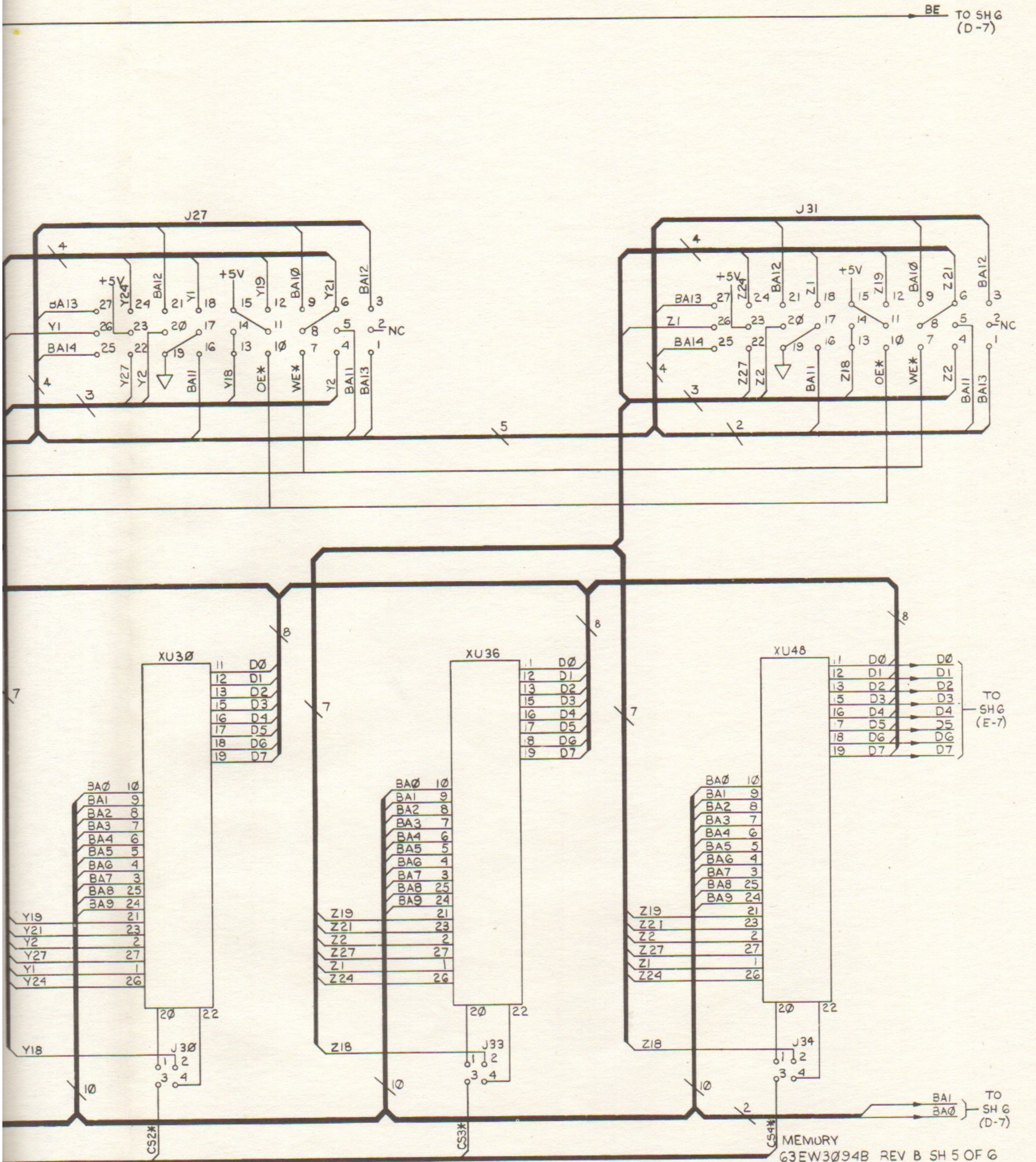
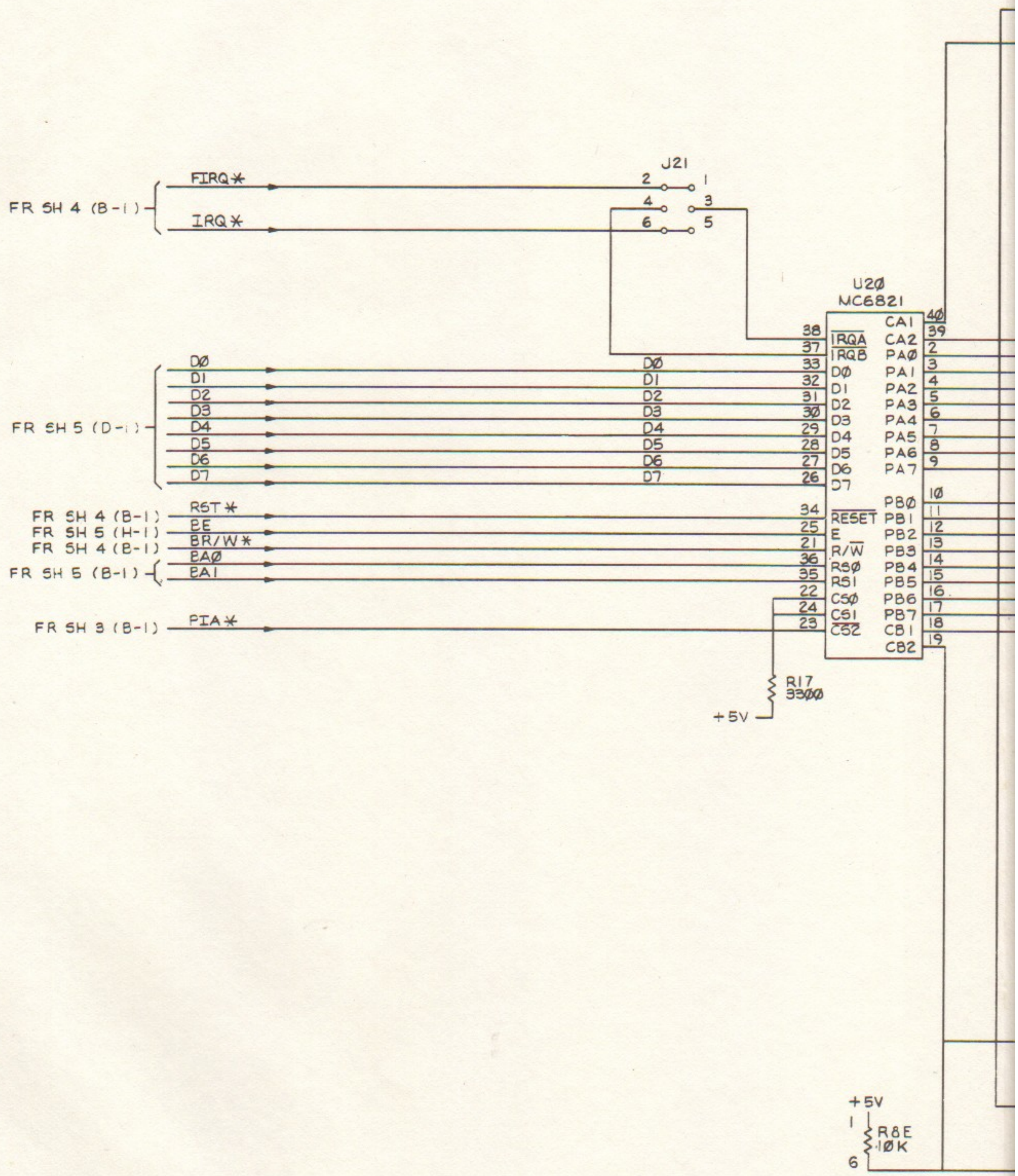
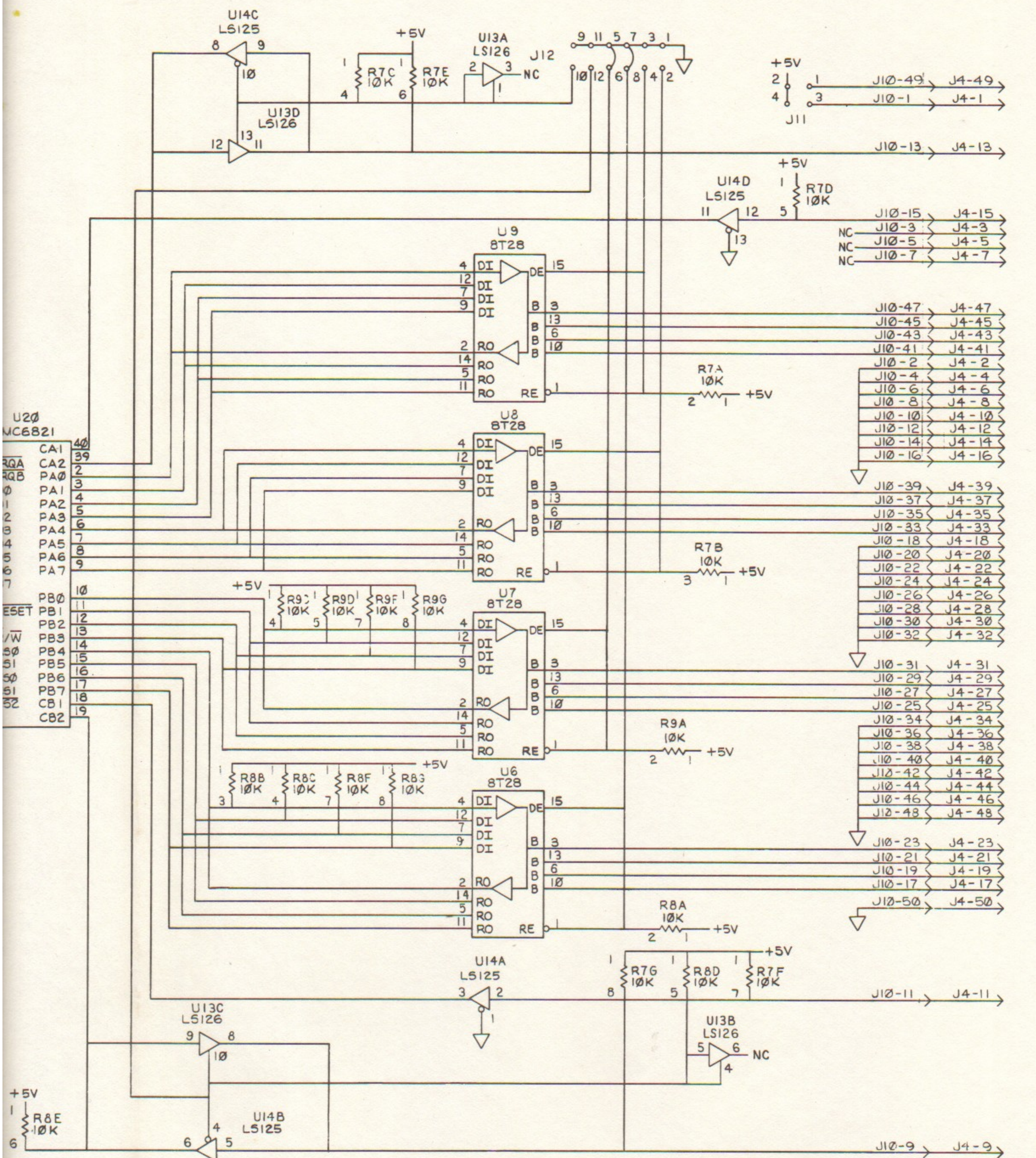


FIGURE 5-2. Micromodule 17 Schematic Diagram (Sheet 5 of 6)


J21
FIRQ*
IRQ*
FR SH 4 (B-1)
U2Ø
MC6821
CA1
CA2
PAØ
PA1
PA2
PA3
PA4
PA5
PA6
PA7
PBØ
PB1
PB2
PB3
PB4
PB5
PB6
PB7
CB1
CB2
IRQA
IRQB
DØ
D1
D2
D3
D4
D5
D6
D7
RESET
E
R/W
RSØ
RS1
CSØ
CS1
CS2
FR SH 5 (D-1)
RST*
BE
BR/W*
BAØ
BA1
FR SH 4 (B-1)
FR SH 5 (H-1)
FR SH 4 (B-1)
FR SH 5 (B-1)
PIA*
FR SH 3 (B-1)
R17
33ØØ
+5V
+5V
R8E
1ØK



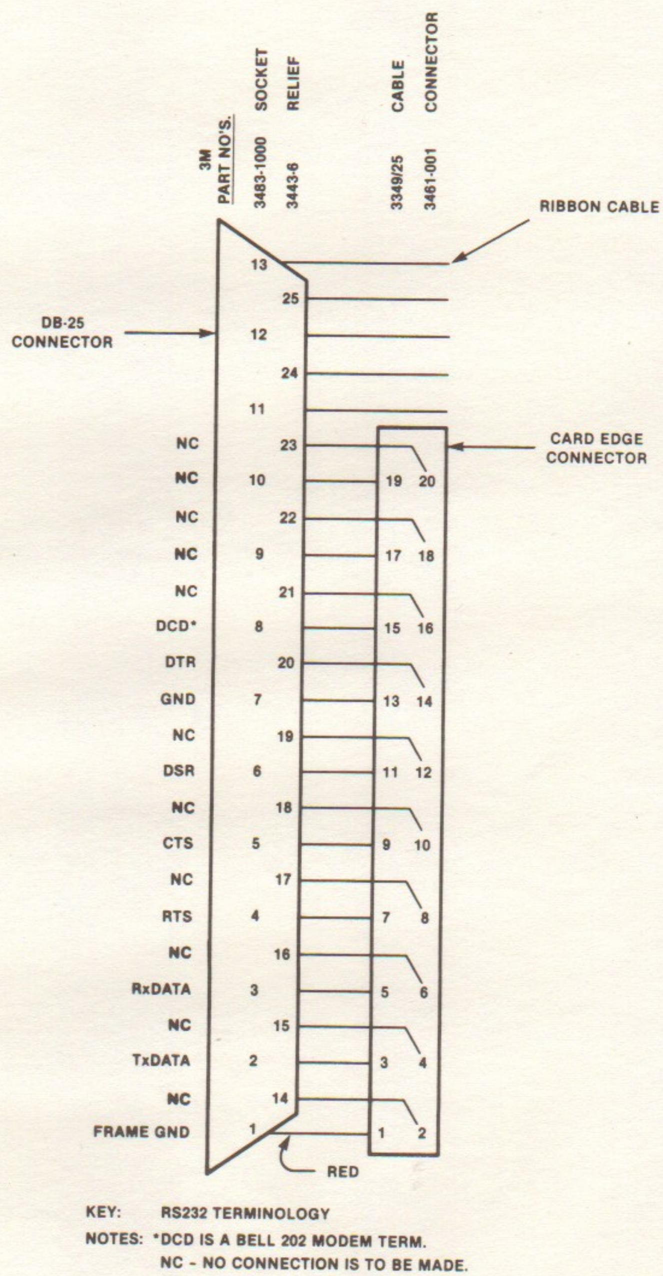
PARALLEL PORT 63EW3Ø94B REV B SH 6 OF 6

FIGURE 5-2. Micromodule 17 Schematic Diagram (Sheet 6 of 6)

APPENDIX A

FABRICATION OF RS-232C SERIAL PORT CABLES

Build the cables to the length desired, per the following figure. Part numbers shown are for 3M company parts, but equivalent ones may be used.



RS-232C Serial Interface Cabling Diagram

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